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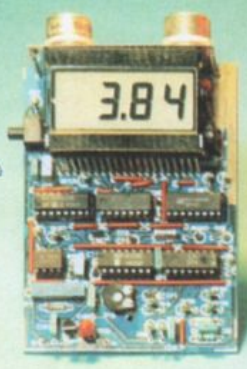

SAM PITRODA
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THE MICRON PROBLEM MAGNIFIED

Two public sector enterprises, Indian Telephone Industries (ITI) and Semiconductor Complex Ltd. (SCL) are aspiring to acquire the 1.5 micron technology. This sophisticated technology is indispensable for future telecommunication equipment.

ITI is keen on importing this technology from the VLSI of USA. SCL, on the other hand, claims that it has already developed two micron technology and with further scaling up of facilities, it would be able to deliver 1.5 micron chip to ITI. Smaller the size and greater the capacity of the chip is the concept behind this technology.

The two organisations are unable to arrive at a common programme and if the ITI proposal is approved, it may cost the nation in foreign exchange worth Rs. 60 crores.

ITI, which is reluctant to join hands with SCL, will have to import semi-processed 1.5 micron chips from VLSI and assemble it at Bangalore. In effect, the hi-tech process would be completed in the USA. For this assembly process and design, ITI has to pay 2.4 million dollars. In the alternative, for complete technology transfer ITI will have to pay 30 million dollars for capital equipment and another 30 million dollars for the manufacturing facilities. In other words, ITI will have to set up a new unit at a cost of Rs. 72 crores.

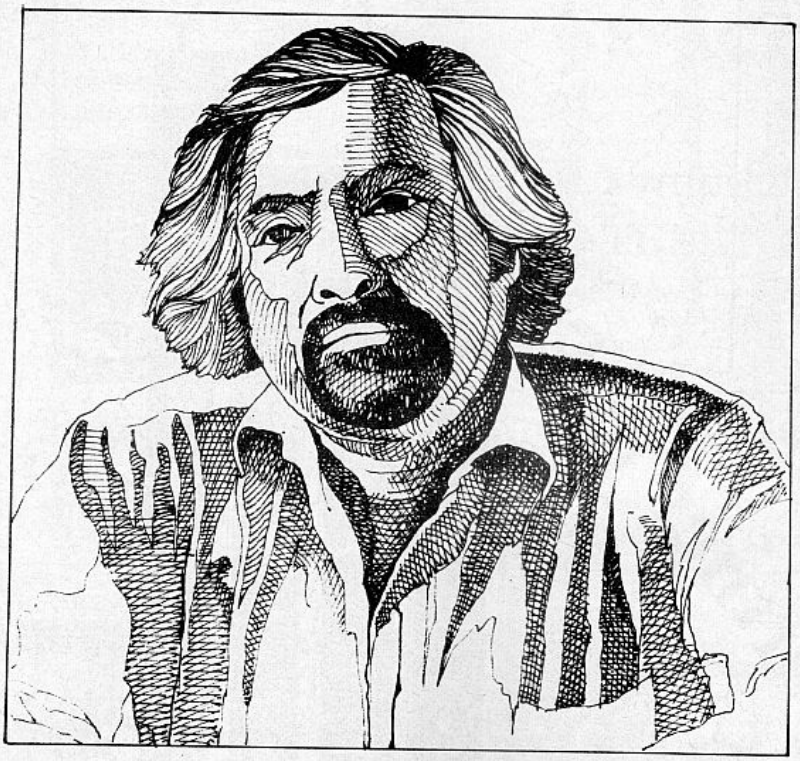
SCL is prepared for a tri-partite agreement involving both the ITI and the VLSI of USA. It is common knowledge that the existing market for chips does not justify another unit while the existing SCL unit can deliver the goods with marginal investment.

The decision here is not beset with any complex issues. Hard-headed, practical decision is called for. ITI and SCL would do well to join hands in mastering the art of miniaturisation.

Front cover

This month, we present a build-it-yourself range finder suitable for measuring distances between 25 cm and 6 metres. It is based on the measurement of the time taken by a sound wave to cover a certain distance.

THE RISE AND RISE OF A MISSIONARY – SAM PITRODA



Some called him the messiah of Indian telecom. Sam wanted himself to be known as Mr. Telecom. Sam Pitroda earned his place in Indian history of development and stays put for completing four other missions, in addition to his own-telecom mission.

After accomplishing the first goal, the Centre for Development of Telematics, in 36 months, with an investment of Rs. 36 crores, the second three-year telecom mission has just completed its first year. This provides an occasion for us to look at the past few months and the future as well, with Sam Pitroda as the centre piece.

The success story of Sam Pitroda in the United States may pale into insignificance before his accomplishments in India in the last four years. Where hot and humid weather conditions prevail with frequent failure of air-conditioning equipment adding to the misery, where stuck up elevator and dead phones are a routine feature, where meeting the deadline of a project is a rare feat and cost overrun is always a rule, Pitroda provided a striking contrast by making possible "the impossible". C-DOT met its target on the dot.

"C-DOT's development of the indigenous switching systems that we have seen are even more important when we look at the manner in which it has been done ... within the stipulated time, without any cost overruns which is within the budgeted amounts, quite unlike other government projects where we seldom see things happening on time and where we seldom even know or have any wild idea of what the cost will be by the time the scheme or project is anywhere near completion". This was the statement of the Prime Minister, Mr. Rajiv Gandhi, when C-DOT made its "Report to the Nation" on October 1, 1987.

If you ask Pitroda what are the achievements of C-DOT, he would not reel out the production of 128-line Rural Automatic Exchange, Private Box Exchange, this product or that product. The real achievement is, says Pitroda, "that we have convinced ourselves that if we can create the right work environment, the right work culture and the right work standards in tune with the needs of our younger people, they can create miracles. That is the achievement. This happens to be in telecom today."

"Everybody said it could not be done. It has been done. May be in real life usage of the equipment, the project got delayed by a few months. When people say, you are late by six months, it is not worth paying attention. We were interested in setting up the process. Product was important because without product, we could not have set up a process. Having initiated the cycle, the more important aspect was the process of delivery and not necessarily the product of delivery."

"We have trained 400 people in C-DOT. We have new work ethics and work standards. The larger question to ask now is whether we can do the same thing in transport sector, energy, water and health."

Pitroda compares the C-DOT as a "bypass surgery in telecom" and it has given rise to the thought if similar bypass surgery can be done in other areas. This is an accomplishment. Of course, there are always spin-offs. One can quote numbers, jobs created, lines manufactured, foreign exchange saved and so on.

Even if decision-makers are willing to do bypass surgery in other areas, the system is not yet ready for that, says Pitroda. By system, Pitroda means these: With Rs. 5,000 in hand, if you want to open a bank account, someone should identify

you. For example, If I want to set up a factory and make a product without any government aid or foreign exchange, why should I need a licence? Take the case of a controller of a commodity which is widely used and needed in industry. When someone suggested that the department of a controller was a misfit now, the question of 400 employees in that office came up. How could they be sacked. Pat came a solution that instead of calling it controller's department, let us make it a "promotion authority". This is what is happening in our system.

"You need a shrewd surgeon to perform bypass. You don't have people like that. Bypass cannot be done by those who are interested in being liked by everybody; being worried about what others might say; wanting to be friendly with the world. Some amount of administrative reform has to come. That is coming as a part of the process but that is still slow", according to Pitroda.

Knowing Pitroda's aversion to foreign technology and desire for self-reliance, it is logical to expect C-DOT to dominate manufacturers in the Indian scene. But, Pitroda disagrees with the idea of dominance. "I am more interested in the process. If a C-DOT licenced manufacturer does something original to the technology we have developed, it is manufacturer's technology. I will be proud to say that it is a great idea."

"If 10 people left C-DOT tomorrow, I expect 50 more to leave. I am not worried. I say it is a healthy sign. I will like 100 people to leave. We have a different perception."

The place for indigenously developed technology in Indian telecom is assured absolutely in the next couple of years. The trend is already set. It is irreversible. That process is over. Those who denounce the trend may belong to vested interests, multinational corporations or those making spare parts or commission agents.

On motivating people, this is what Sam says: What I try to do is basically to articulate the objectives, give them clarity of purpose, give them a long-term vision, see how they get fixed-in and break up their task into manageable, tangible, deliverable milestones. I give them hope and kill cynicism. I kill cynicism and sometimes overdo it."

Sam Pitroda does not meddle with the day to day problems of C-DOT anymore. He does not even know what his people are doing. For example, the 1988 plan was prepared by his colleagues. He made a few comments here and there. On October 1, they began the planning process for 1989. Lot of discussions and debate, gyrations and commotion take place before the document is prepared. The C-DOT plan document is distinctly different from the rest. It has only two things-activity with date and the name of the persons who will do the job. Later, in July next, the plan progress will be reviewed.

Some major C-DOT accomplishments

August 1984: C-DOT starts work on digital switching in India.

July 1985: First call placed through PBX in laboratory.

August 1985: Inauguration of 128-port PBX takes place.

September 1985: PBX demonstrated to Prime Minister.

March 1986: Rural exchange (RAX) installed at Kittur field trial site.

May 1986: RAX cutover takes place at Kittur.

September 1986: C-DOT participants in Africa Telecom 87 at Kenya.

December 1986: Manufacturers' associations formed.

January 1987: Agreement signed with ITI to transfer RAX technology.

February 1987: C-DOT participates in Indiacom 87 in New Delhi.

March 1987: 10,000 calls simulated on main exchange (MAX); Second C-DOT telecom mission approved.

May 1987: RAX installed at Churhat.

June 1987: MAX installed at field trial site in Delhi.

July 1987: RAX phase II DOT evaluation commences.

August 1987: 5000-port MAX demonstrated at Ulsoor; inauguration of ITI/C-DOT factory takes place; C-DOT completes first technology mission; participation by C-DOT directors and Sam Pitroda in the South Asian Association for Regional Cooperation (SAARC).

September 1987: Second technology mission commences.

The claim of indigenisation, invariably elicits a query on the indigenous content in a product or project. Pitroda, rightly, spurns such mundane definition of indigenisation. "what is the definition of indigenisation? Is it only applicable to parts? Let us say, the bill of a product is 100 dollars. It has 50 dollars worth of material brought from abroad. Does it mean, 50 per cent indigenisation? This 100 dollar could give rise to 700 dollar worth of products. Installation, cabling, maintenance engineering and so on also constitute a part of the project. The percentage would not mean anything."

Today, in C-DOT system, roughly 40 per cent of the components are imported and most of them are ICs. In six months. Semiconductor Complex Ltd. will produce them. Then, the import content will be less than 10 per cent which will be microprocessors and memory.

The C-DOT system is to be manufactured by nearly two dozen companies. There is a competition now. In, the past... it was a seller's market. As soon as a system was produced, there was someone to lift and the price was dictated by the manufacturers. C-DOT has changed the situation. The price for a line was around Rs. 5,000 before and it has now come down to Rs. 2,400.

The media has made much about Pitroda's aversion to the introduction of the cellular telephone in India. What exactly are his views? Explains Pitroda: "Let us not confuse cellular phone with car phone. Car phone is something we do not need in this country at this stage. In a country with 250 district headquarters which are not connected to STD, how can you afford to give 5000 people the car phone? The system around me is not efficient. Then, how can I be efficient? The train may not arrive in time. The driver may not come on time. My meeting will begin 20 minutes late. So, the system has to be in tune with the field. We are not ready yet to have the car telephone. With car telephone now, the only thing I can do is to tell my wife I will be late for dinner. Money can be better spent elsewhere."

CENTRONICS INTERFACE FOR SLIDE FADER

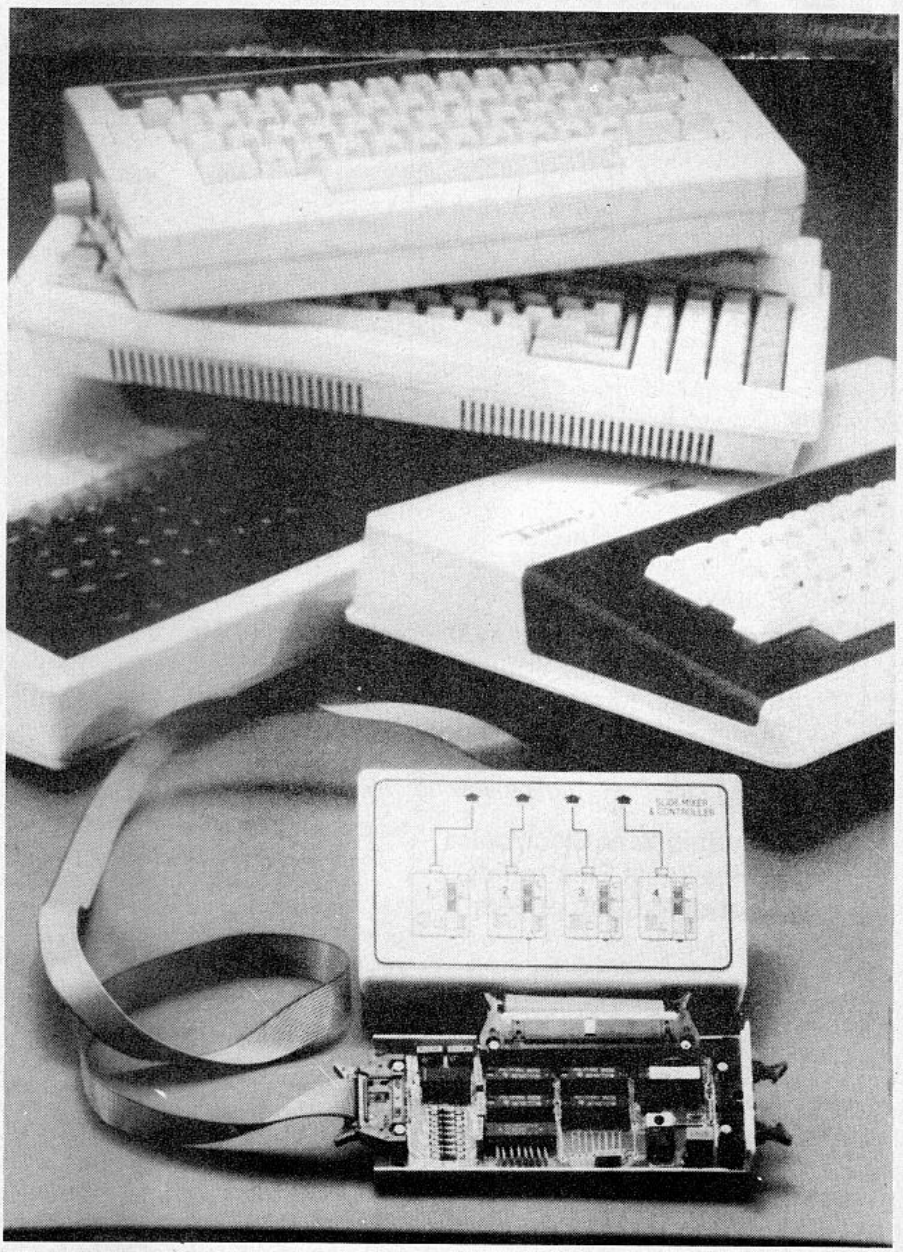
The slide fader published earlier this year was originally designed for use with MSX computers. To further boost the interest in this versatile and simple-to-build circuit, an interface was developed that allows the fader to be driven from a standard Centronics port, which is available on practically any type of home computer.

The slide fader discussed in Ref. [1] is a computer peripheral that makes it possible to control up to four slide projectors independently. Slide carriage control (forward/reverse) and lamp intensity (in 64 steps) are programmable on the computer. To keep the operation of the circuit as simple as possible, one 8-bit output port is, in principle, required for each projector. The interface circuit described here effectively extends the number of ports from one to four. One Centronics port can drive up to four interfaces of the type described here, so that the computer can program up to 16 individual slide projectors.

The Centronics port: universal and flexible

The Centronics parallel printer port is an input/output connection composed of 8 data lines, two ground connections, 3 handshake lines and a number of other lines for printer control. Virtually any modern (home-) computer is equipped with a Centronics outlet, whose pinning and handshake protocols have gained worldwide acceptance. On IBM PCs and compatibles, the Centronics port is usually identified as LPT1:.

The timing diagrams of Fig. 1 show two handshaking arrangements on the Centronics port. In the so-called STROBE/ACK ('normal') protocol, the peripheral device activates $\overline{\text{ACK}}$ (acknowledge) after reception of the rising edge of the $\overline{\text{STROBE}}$ signal supplied by the computer. This is not allowed to send new data to any peripheral connected to the port, before it has received the $\overline{\text{ACK}}$ pulse. When the peripheral has processed the data, it indicates readiness to accept new data by making $\overline{\text{ACK}}$ logic low. Some computers work with the STROBE/ACK protocol, some with the slightly more complex STROBE/ACK/BUSY protocol, while



Now all computers sporting a Centronics outlet can be connected to the powerful slide fader published earlier this year.

still others can handle both. The interface circuit described here has been designed to support both handshaking protocols.

Port expansion: from one to four

Briefly recapitulating the operation of the slide fader, the 8-bit dataword it receives from the computer is composed of three functional blocks:

- databits D0 to D5 to determine the lamp intensity in 64 (2^6) steps;
- databit 6 to control the loading of the slides, and the reverse movement of the carriage;
- databit 7 for the same function, but in forward direction.

D6 and D7 are never logic one at the same time. This combination, however, makes it possible to design a circuit that distinguishes between a projector dataword and a projector selection word. With D6 and D7 both logic high in the 8-bit dataword sent to the slide fader, 6 bits remain to select up to 16 projectors. Figure 2 shows that databits D2 through D5 in the projector selection word are used for selecting projector 1, 2, 3 or 4. Note that these are off when the associated bit is logic high. When more than one projector is selected at a time, all of these receive the same dataword. The two remaining bits, D0 and D1, are used for selecting one of four projector blocks.

Circuit description

With reference to the circuit diagram in Fig. 3, IC_4, IC_5, IC_6 and IC_7 form the 8-bit output ports that control one slide projector each. The interface is connected to the Centronics outlet of the computer via connector K_1. R-C low-pass networks at the inputs of data buffer IC_3 suppress interference on the datalines. IC_3 is permanently selected because its enable inputs, $\overline{G2}$ and $\overline{G1}$, are hard-wired to ground. Bistable FF_1 is set by the $\overline{STROBE}$ pulse, so that BUSY

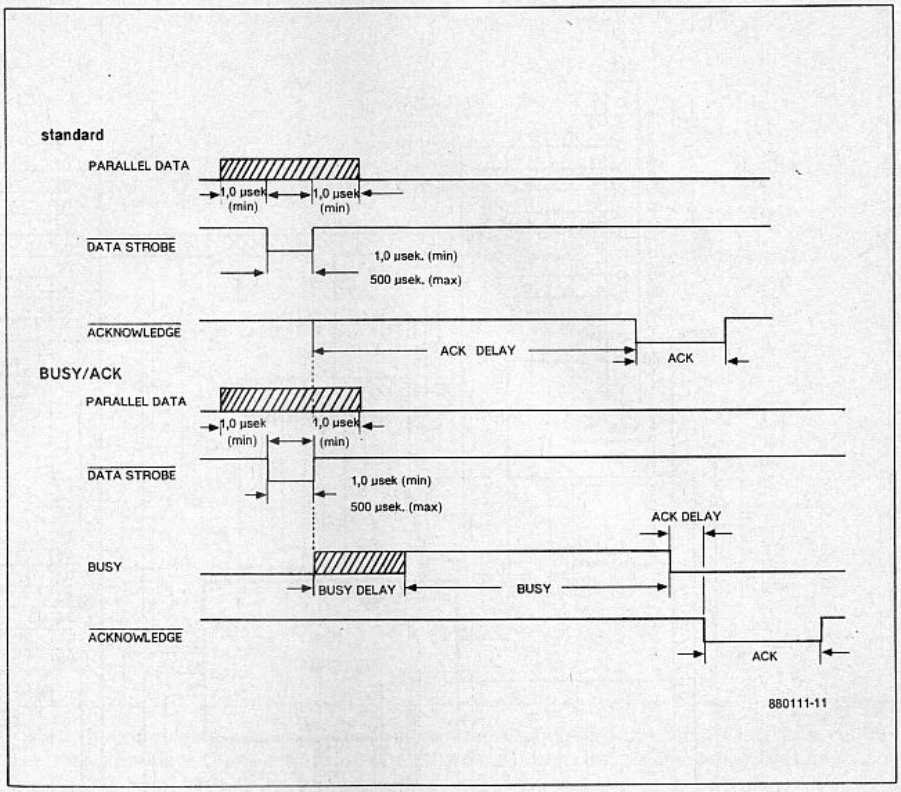


Fig. 1. Basic timing of the two handshaking arrangements commonly used on the Centronics port.

is activated via output Q. Output $\overline{Q}$ goes low and discharges C_1 via R_2. After a predefined period, the level at input $\overline{CLEAR}$ is sufficiently low for the bistable to be reset. Output Q toggles and de-activates BUSY, while C_1 is charged again by the logic high level provided by output $\overline{Q}$. The rising edge of $\overline{Q}$ triggers a second bistable, FF_2, whose operation is similar to that of FF_1. The short, negative-going, pulse at the $\overline{Q}$ output forms the $\overline{ACK}$ signal for the computer. The fixed handshake timing used here is fairly crude, but this is of little consequence in practice, since the speed of the circuit allows it to latch data on the negative edge of the STROBE signal. This is in contrast to a printer, which often needs considerably more time to transfer the information on to paper.

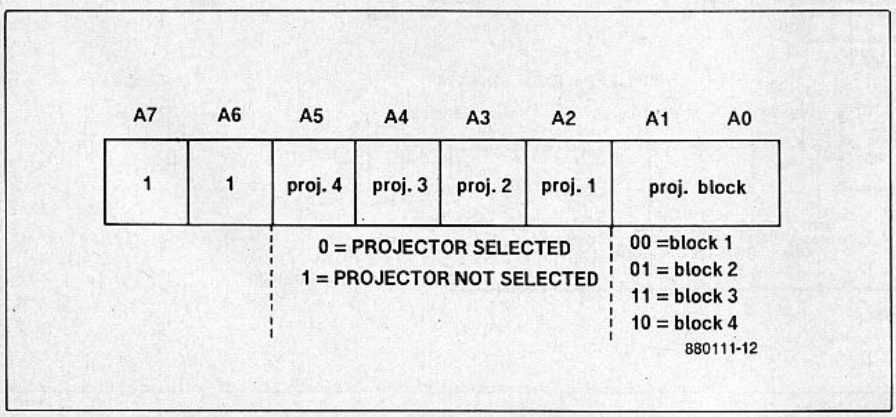


Fig. 2. Bit assignment in the projector selection word (D6 = D7 = 1). One byte allows selecting 4 of 16 slide projectors.

Connector K_2 allows up to four interface circuits to be chained, so that up to 16 projectors can be controlled. Components IC_2, R_2, R_3, C_1 and C_2 are only required on the first interface in the chain, i.e., the one connected to the computer's Centronics port. K_2 carries 8 buffered databits, X0 and $\overline{X1}$, ground, and the $\overline{STROBE}$ pulse.

The PAL (programmable array logic) in position IC_1 combines the functions of a number of digital integrated circuits, and thus keeps the chip-count of the circuit relatively low. This, in turn, economizes on board space. Figure 4 shows the internal configuration, after programming, of PAL Type 16R4 (this is available ready-programmed through the Readers Services). The chip combines databits D0 through D7 with the $\overline{STROBE}$ pulse to generate the clock signals for latches IC_4, IC_5, IC_6 and IC_7, and also separates projector datawords from projector selection words. This is done by gates N_7 through N_{10} in the PAL. Databits D6 and D7 are applied to pins X6 and X7. As already discussed, the difference between a dataword and a selection word is that in the latter D6 and D7 are both logic high. If this is so when $\overline{STROBE}$ goes low, the output of N_{10} will remain logic high. It does not go low until D6 and D7 are simultaneously logic low, or of complementary logic level.

The output of N_{10} controls three-state buffers internal to the 16R4. During the transmission of a projector selection word, buffer N_2 is enabled, so that the

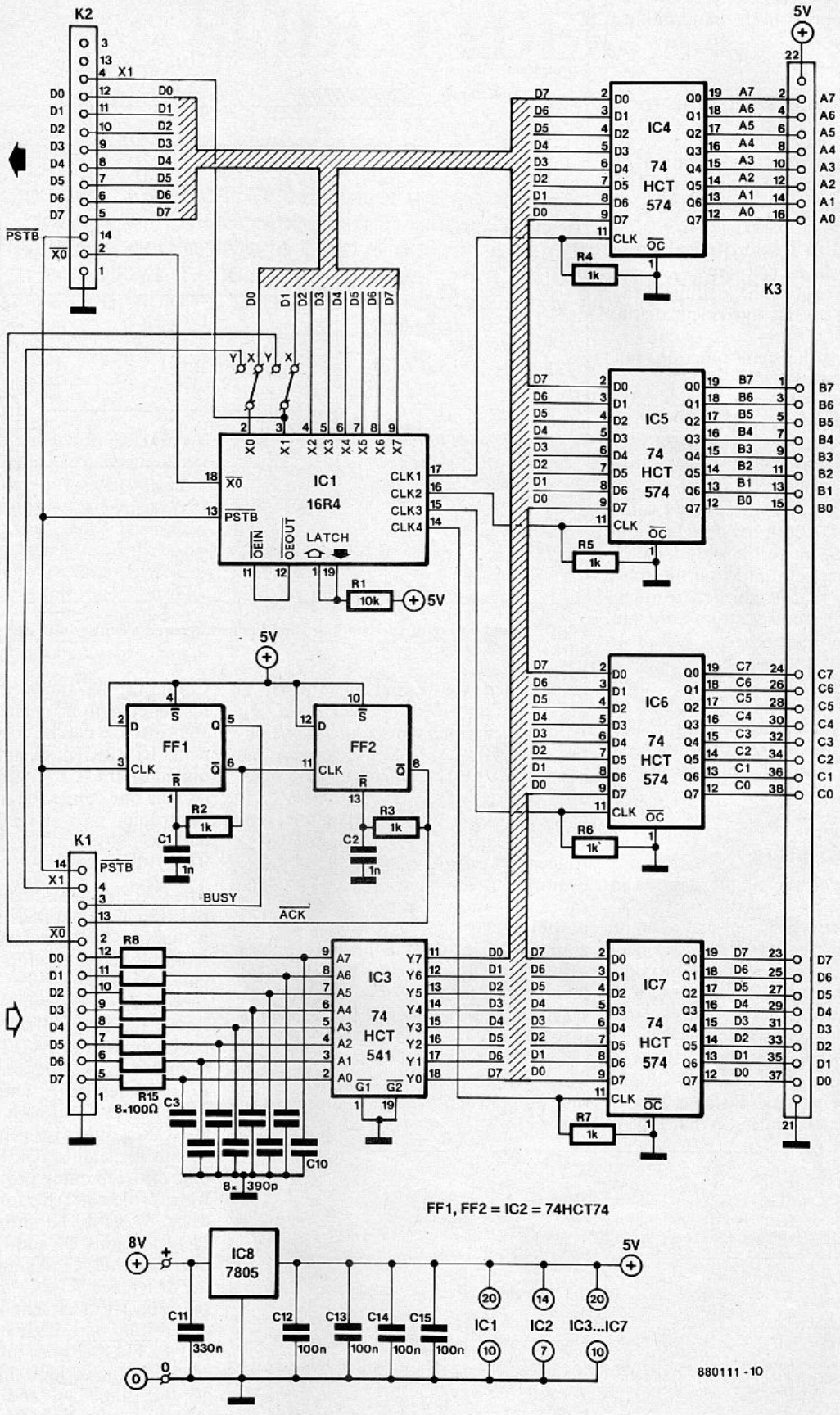


Fig. 3. Circuit diagram of the interface that makes it possible to drive the slide fader from any computer equipped with a Centronics outlet. A ready-programmed PAL, IC1, keeps the chip-count as low as possible.

output of N_{11} is logic low. Output buffers N_{12} through N_{15} then block the output signals of the four bistables, so that the clock inputs of the registers in the interface circuit are held logic low by pull-down resistors R_4 through R_7. The four bistables, however, load the data applied to the D input. Since both the output of N_{11} and inputs X1-X2 of the selected interface board are logic low, the values of variables X2, X3, X4 and X5 determine the projector selection.

X0 and X1 are the two bits that select one of four interfaces. For the first module, the combination is D0=0 and D1=0. To select a projector, the D-input of the relevant bistable in the PAL should go logic low, so that the Q output follows this level after a clock pulse. When the dataword is sent, the output of N_{16} goes logic high, and the output state of each of the 4 bistables is transferred to the clock input of the associated register on the interface board. A logic high level at an output Q causes a positive-going clock pulse (CLK) that enables the relevant register to latch data from the databus. Any dataword that follows immediately, e.g., a carriage return (CR) code sent by the computer, simply does not reach the slide fader. The projector selection is erased during the writing of a dataword. Three-state buffer N_2 is switched to high impedance via N_{10}, and its output is logic high due to pull-up resistor R_1. Data is read via the D inputs, and the Q outputs of the bistables follow the data level. This means that it is impossible for a second positive edge to appear on the CLK output of the Centronics interface when a second dataword is being sent. Any projector dataword should, therefore, be preceded by a projector selection word. It is not possible to send two successive datawords.

To select a Centronics interface card, both X0 and X1 should be logic low. Selective addressing of one-of-four interfaces is achieved by swapping and inverting X0 and X1 on each module as shown in Fig. 5. The selection codes for cards 1, 2, 3 and 4 are 00, 01, 11 and 10 respectively.

Finally, constructors in possession of a PAL programmer will find the data for loading the 16R4 in Fig. 6.

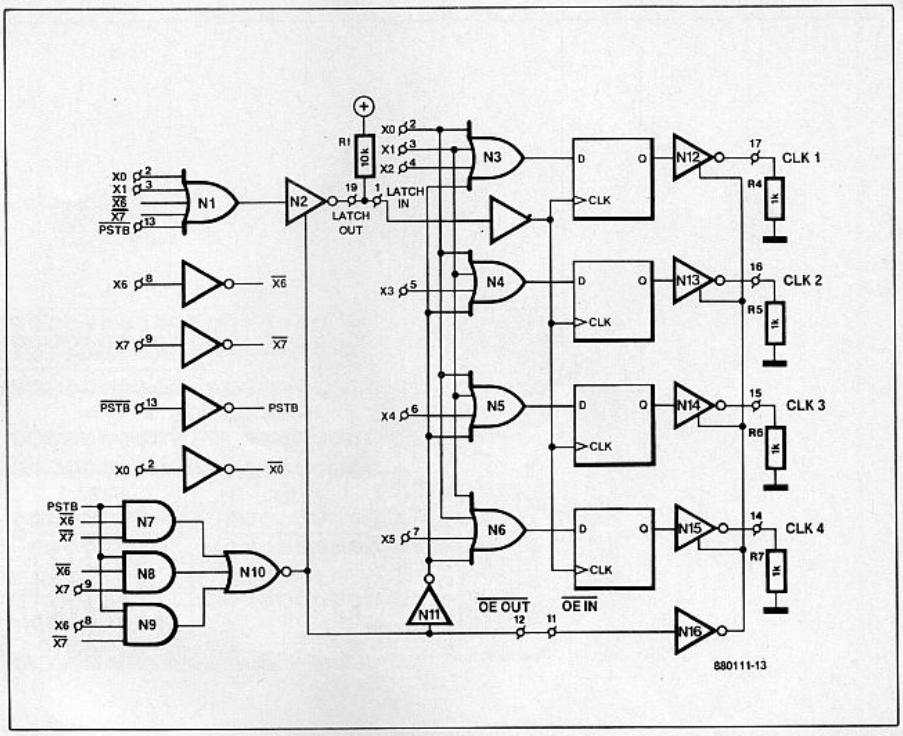


Fig. 4. Internal configuration of the programmed PAL Type 16R4 for the interface circuit. The PAL combines the functions of at least half a dozen discrete integrated circuits.

Construction

Figure 7 shows the compact printed circuit board designed for the Centronics-to-slide fader interface. Start the construction with fitting the wire links. Connect the two points marked **A** with an insulated wire, and do the same with the two points marked **B**. The jumper block below IC_1 is best made from a 6-way straight PCB header and two jumpers. On module 1, install the two jumpers in positions X, on the other modules in positions Y. K_1 and K_2 are 14-way, male, angled, headers with eject handles, secured on to the PCB with the aid of short M2 bolts and nuts. K_3 is a similar header with 50 pins. It may be omitted when the Centronics interface card is fitted on to the slide fader card — in that case, connect the two cards with a short length of 50-way flatcable

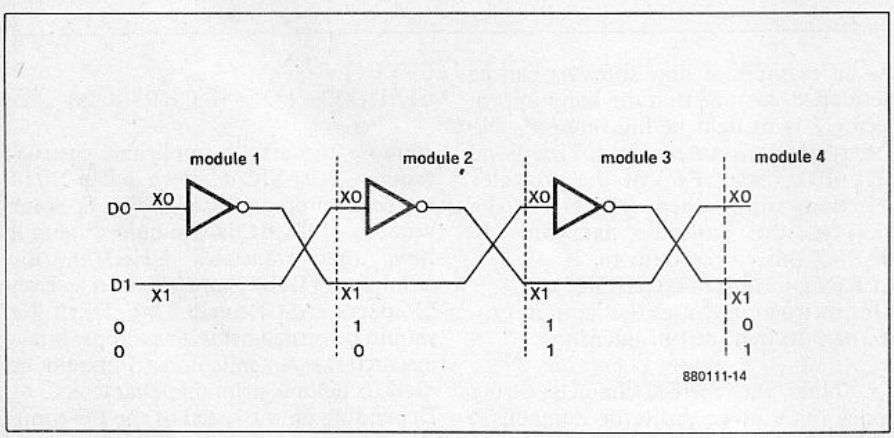


Fig. 5. Up to four Centronics interface cards can be addressed individually by connecting them in series, and swapping and inverting the X0-X1 selection lines.

```
DEVICE 16R4

LATCHIN     1
A0          2
A1          3
A2          4
A3          5
A4          6
A5          7
A6          8
A7          9
GND         10
/OEIN       11
/OEOUT      12
/PSTB       13
CLK4        14
CLK3        15
CLK2        16
CLK1        17
NEXTA0      18
LATCHOUT    19
VCC         20

MACRO F0 PSTB*/A6*/A7;
MACRO F1 PSTB*A6*/A7;
MACRO F2 PSTB*/A6*A7;

START

/OEOUT          /=&F0+&F1+&F2;
CLK4            /:=A5+A0+A1+OEOUT;
CLK3            /:=A4+A0+A1+OEOUT;
CLK2            /:=A3+A0+A1+OEOUT;
CLK1            /:=A2+A0+A1+OEOUT;
NEXTA0          /=A0;
LATCHOUT        /=/PSTB+/A6+/A7+A0+A1;
LATCHOUT.ENA    =/OEOUT;

END                                 880111-15
```

Fig. 6. Programming information for PAL 16R4. This chip is available ready-programmed through the Readers Services.

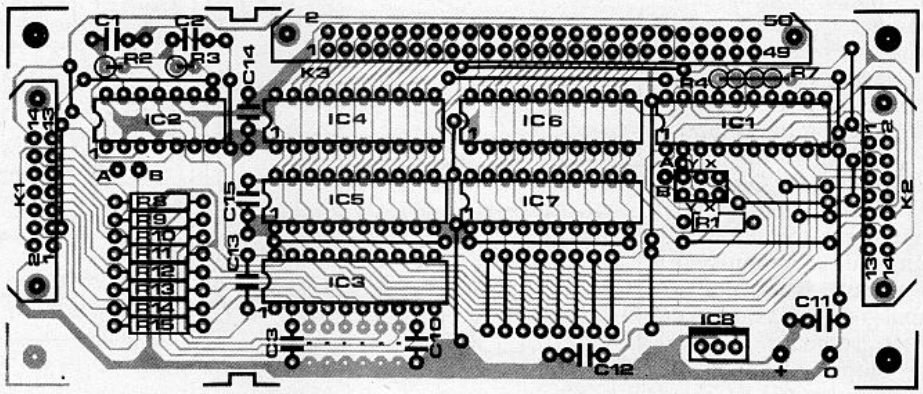


Fig. 7. Compact single-sided printed circuit board for the interface card.

PARTS LIST

Resistors (±5%):
R1 = 10K
R2 . . . R7 incl. = 1K0
R8 . . . R15 incl. = 100R

Capacitors:
C1;C2 = 1n0
C3 . . . C10 incl. = 390p
C11 = 330n
C12 . . . C15 incl. = 100n

Semiconductors:
IC1 = 16R4

IC2 = 74HCT74
IC3 = 74HCT541
IC4 . . . IC7 incl. = 74HCT574
IC8 = 7805

Miscellaneous:
S1;S2 = jumper.
6-way (2 × 3-pin) straight PCB header to form jumper block.
K1;K2 = 14-way angled PCB header (male; with eject handles; raster 0.1 in.; 2 rows).
K3 = 50-way angled PCB header (male; with eject handles; raster 0.1 in.; 2 rows).
Enclosure: e.g. Heddic 222. Available from Chartland Electronics Limited • Chartland House • Twinoaks • COBHAM KT11 2QW. Tel.: 037 284 2553).
PCB Type 880111 1

Note: Some constructors of the slide fader have found the Type TCA280A lamp dimmer circuit difficult to obtain. The chip is available, however, from C-I Electronics • P.O Box 22089 • 6360 AB Nuth • The Netherlands

soldered direct to the PCB connections. The Centronics interface is conveniently powered from a mains adaptor capable of supplying 8 to 10 VDC at about 250 mA.

Software: the finishing touch

Programming the slide fader via the Centronics interface described here requires sending two successive characters — first the projector selection word, then the projector dataword. The LPRINT command available in BASIC is eminently suited to controlling the slide interface, because it provides a direct route to the Centronics port.

As an example of how software can be developed, assume that the lamp in projector 2 is to light at full intensity. No other functions are required. First, send 1111 0100_2 (244_D; $F4_H$) as the projector selection word, then 0011 1111 (63_D; $3F_H$) as the projector dataword. In BASIC, this corresponds to

LPRINT CHR$(244);CHR$(63).

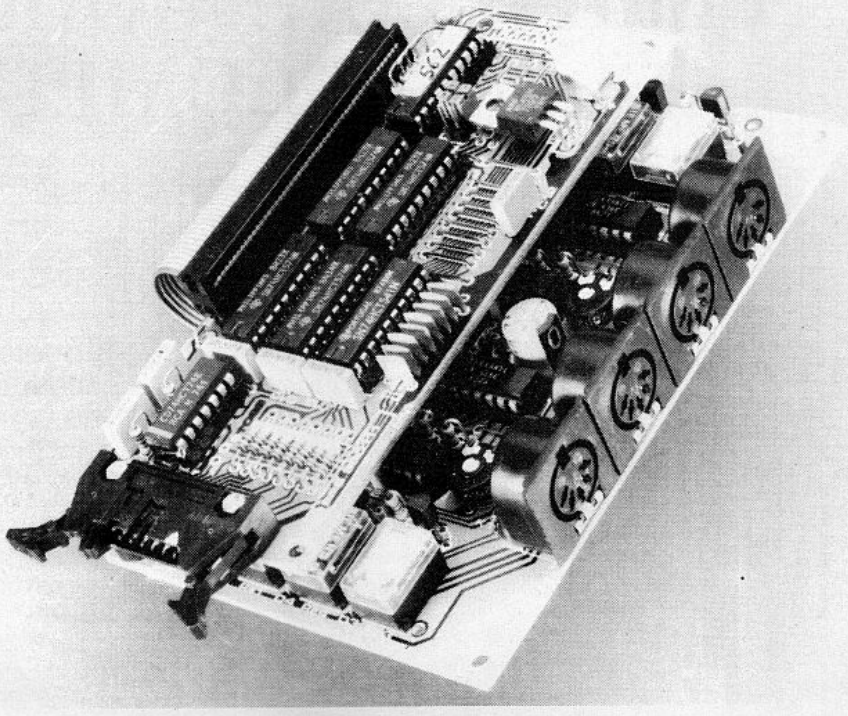
This instruction causes the lamp in projector 2 to light at full intensity.

To obtain the correct character-string codes for a given projector number, P, and block number, B, use the equation:

LPRINT
CHR$(252−4*2^P+B);CHR$(data)

A more universally applicable instruction in GWBASIC is shown in line 210 of the demo program listed in Fig. 8. Some versions of BASIC have a built-in output filter that translates CHR$(9), the tabulation (TAB) character, into a series of spaces (ASCII code 32_D). This filter should be turned off with an appropriate instruction. A semicolon (;) should be used to delimit printable characters.
Depending on the speed of the PC running the demo program of Fig. 8, and the type of slide projector used, it may be necessary to assign different start values

to variables S (dissolve speed), F, R and T (carriage movement). Use different values for F and R to enable using projectors with single-key control. All projectors used are identified in hexadecimal notation in string A$ (line 40).



Prototype of the Centronics interface secured on top of the slide fader board.

```
10 ' Automatic dissolve program for CENTRONICS to SLIDE CONTROLLER interface
20 '
30 CLS : LOCATE 5,10
40 A$="0123": PRINT "The projectors selected are ";A$
50 LOCATE 8,10: PRINT "[ SPACE ] for next projector"
60 LOCATE 9,10: PRINT "[ ENTER ] for previous projector"
70 LOCATE 11,10: PRINT "[ F ] for fast dissolve"
80 LOCATE 12,10: PRINT "[ N ] for normal dissolve"
90 LOCATE 13,10: PRINT "[ L ] for long dissolve"
100 B$=""
110 IF LEN(A$)>16 OR LEN(A$)=0 THEN GOTO 700
120 '
130 FOR I=1 TO LEN(A$)
140     B=ASC(MID$(A$,I,1))
150     IF B<48 OR B>102 THEN 700
160     IF B<58 THEN B=B-48: GOTO 210
170     IF B<65 THEN 700
180     IF B<71 THEN B=B-55: GOTO 210
190     IF B<97 THEN 700
200     B=B-87
210   B=252-2*(B MOD 4)+4+B\4 +(B\4=3)*(B\4=2)
220   B$=B$+CHR$(B)
230 NEXT
240 '
250 LPRINT CHR$(192);CHR$(193);CHR$(194);CHR$(195);CHR$(0)          ' All projectors off
260 '
270 F=200:                                                          ' Initialize constants
280 R=400:                                                          ' Forward changing time
290 T=1000:                                                         ' Reverse changing time
300 S=250:                                                          ' Total changing time
310 '                                                               ' Basic dissolve speed
320 X=0: Y=0: L=LEN(A$)-1                                           ' Main loop
330 I$=INKEY$ : IF I$="" THEN 330
340   IF I$=" " THEN GOSUB 400
350   IF I$=CHR$(13) OR I$="r" OR I$="R" THEN GOSUB 490
360   IF I$="f" OR I$="F" THEN D=S
370   IF I$="n" OR I$="N" THEN D=2*S
380   IF I$="l" OR I$="L" THEN D=3*S
390 GOTO 330
400 '                                                               ' Next projector
410 Y=X
420 X=ASC(LEFT$(B$,1))
430 A$=RIGHT$(A$,L)+LEFT$(A$,1)
440 B$=RIGHT$(B$,L)+LEFT$(B$,1)
450 GOSUB 580
460 LOCATE 15,10: PRINT "Projector ";RIGHT$(A$,1);" is on
470 DA=128: C=F: GOSUB 640
480 RETURN
490 '                                                               ' Previous projector
500 DA=64: C=R: GOSUB 640
510 Y=X
520 A$=RIGHT$(A$,1)+LEFT$(A$,L)
530 B$=RIGHT$(B$,1)+LEFT$(B$,L)
540 X=ASC(RIGHT$(B$,1))
550 GOSUB 580
560 LOCATE 15,10: PRINT "Projector ";RIGHT$(A$,1);" is on
570 RETURN
580 '                                                               ' Dissolve
590 FOR I=0 TO 63
600 LPRINT CHR$(X);CHR$(I+(I=9));CHR$(Y);CHR$(63-I+(63-I=9))
610 FOR J=0 TO D: NEXT
620 NEXT
630 RETURN
640 '                                                               ' Change slide
650 LPRINT CHR$(Y);CHR$(DA)
660 FOR J=0 TO C: NEXT:                                             ' changing time
670 LPRINT CHR$(Y);CHR$(0)
680 FOR J=0 TO 1000:C: NEXT:                                        ' Wait before next dissolve is allowed
690 RETURN
700 CLS: LOCATE 9,10: PRINT "Error in line 30 adjust A$"
710 END
```

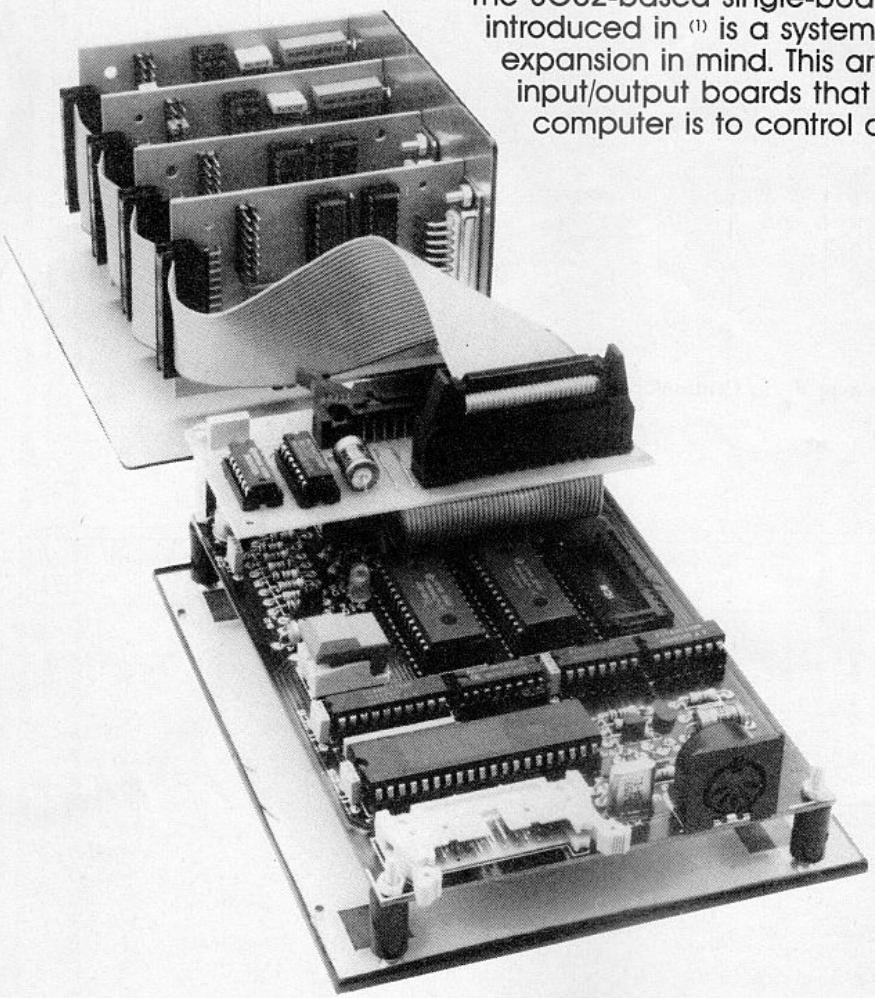
880111-16

Fig. 8. This demonstration program for the Centronics interface has been written in GWBASIC, so that it can run on all IBM PCs and compatibles. For other computers, some syntactical changes may be required. Read the text on the start values of variables S, F, R and T.

PERIPHERAL MODULES FOR BASIC COMPUTER

from an idea by J. Haudry

The 8052-based single-board process and control computer introduced in [1] is a system designed with hardware expansion in mind. This article describes two modular input/output boards that are indispensable when the BASIC computer is to control digital or analogue peripherals.



Just for those who do *not* know: the system described in reference [1] is a single-board computer based on Intel's Type 8052AH-BASIC v1.1 microcontroller. As indicated by the type number, the computer can be programmed in BASIC. Programming is done with the aid of a dumb terminal (or a host computer running a terminal emulation program), and a bidirectional RS232 link to the BASIC computer. The system can run programs from an on-board EPROM, and is, therefore, ideal for small-scale process and control applications ('turnkey' systems). Interestingly, control software is written and debugged direct on the system, and loaded into EPROM by the CPU, i.e., without the need of an EPROM programmer.

The BASIC computer has been one of the most popular projects published over the last year or so in this magazine. Users have found it simple to build, program, and connect to existing equipment. The BASIC interpreter in the 8052AH-BASIC is relatively fast, and supports a number of extremely useful bit-manipulation commands. Machine code programming is also possible when the Intel reference guide is available.

After our publishing of the 'bare bones' of the BASIC computer, many users have expressed a firm interest in input/output extensions for connection to the available bus. The modules described here are our answer to these requests. Readers may be interested to know that the modules are also compatible with a 8751-based autonomous input/output controller with RS232 interface, to be described in a forthcoming issue of this magazine.

Peripheral modules for BASIC computer.

Technical characteristics:

- Modular I/O system comprises one address decoder/interface, and one or more input and/or output modules.
- Parallel mounting of up to eight digital I/O modules.
- Analogue output module based on 10-bit DAC supplies accurate voltage for control applications. Voltage span: 0 to 10.23 V, programmable in 10 mV steps.
- Use of one or more analogue output modules restricts the maximum number of modules controlled by 1 address decoder/interface to 7.
- Maximum of 2 address decoder/interface boards enables control of up to 16 digital I/O modules, or 14 analogue output modules.
- Power digital outputs sink up to 500 mA at 50 V. Maximum total dissipation of output driver; 2.25 W (dissipation is 0.5 W, for example, when 300 mA is supplied).

Functional description of the I/O modules

Two types of bus-connected module are described here:

- a bidirectional digital interface with 8 inputs and 8 buffered outputs;
- an analogue output module capable of supplying a highly accurate output voltage between 0 and +10.23 V, in steps of 10 mV.

Between the BASIC computer's bus and these modules sits a simple address decoder. The I/O modules are small units, and one address decoder allows parallel connection of up to 8 digital modules, or up to 7 modules when analogue and digital types are used simultaneously. The BASIC computer itself allows the connection of a maximum of two address decoders. The modular structure of the expanded BASIC computer is illustrated in the block diagram of Fig. 1. The address decoder provides a bus in the form of a flatcable, which runs from one I/O module to the next.

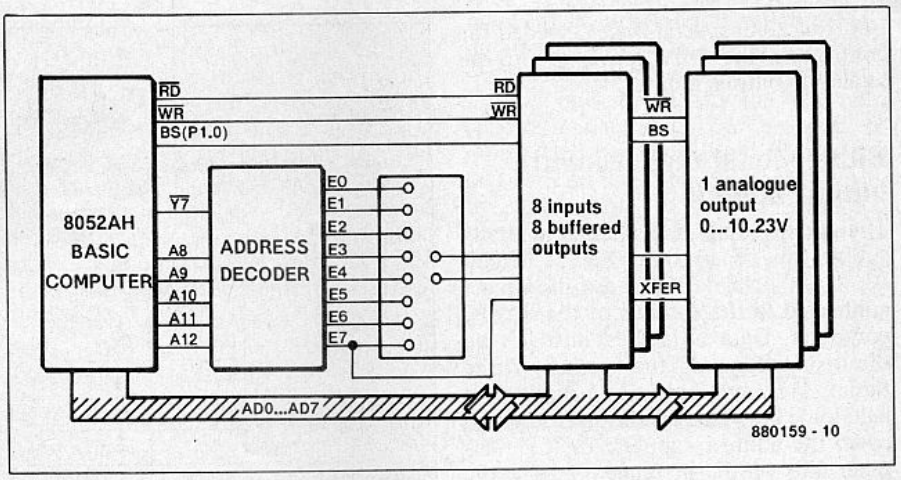


Fig. 1. The input/output system for the BASIC computer is a modular structure that gives the user freedom of configuration. The I/O boards are connected direct to the databus of the microcontroller, but are addressed in the memory segment reserved for peripheral circuits.

Address decoder for I/O modules

The circuit diagram of Fig. 2 shows the simplicity of the address decoder for the I/O modules. Monostable IC_2 is used for timing one of the control signals for the 10-bit digital-to-analogue (D-A) converter.

The presence of address lines A11 and A12 allows defining two address ranges, so that two decoders can be mounted in parallel, each with a different jumper configuration (A-D). Table 1 shows that each card occupies 256 addresses.

Address decoder IC_1 supplies 8 enable signals, $\overline{E0}$ to $\overline{E7}$. The special use of $\overline{E7}$ on the analogue output module will be reverted to, as well as the function of signal BS, which is supplied direct by the BASIC computer, and runs to the analogue output board(s) via the address decoder board.

Monostable IC_2 changes the timing of $\overline{WR}$ to provide a signal called $\overline{SWR}$

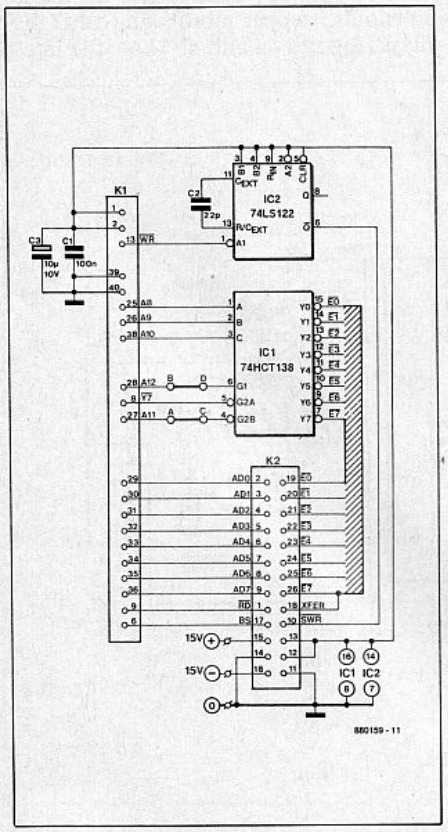


Fig. 2. The interface shared by the I/O modules is composed of an address decoder that divides the available memory space for I/O in 8 blocks of 256 addresses, and a circuit that modifies the timing of the WR pulse to ensure correct loading of the D-A converter.

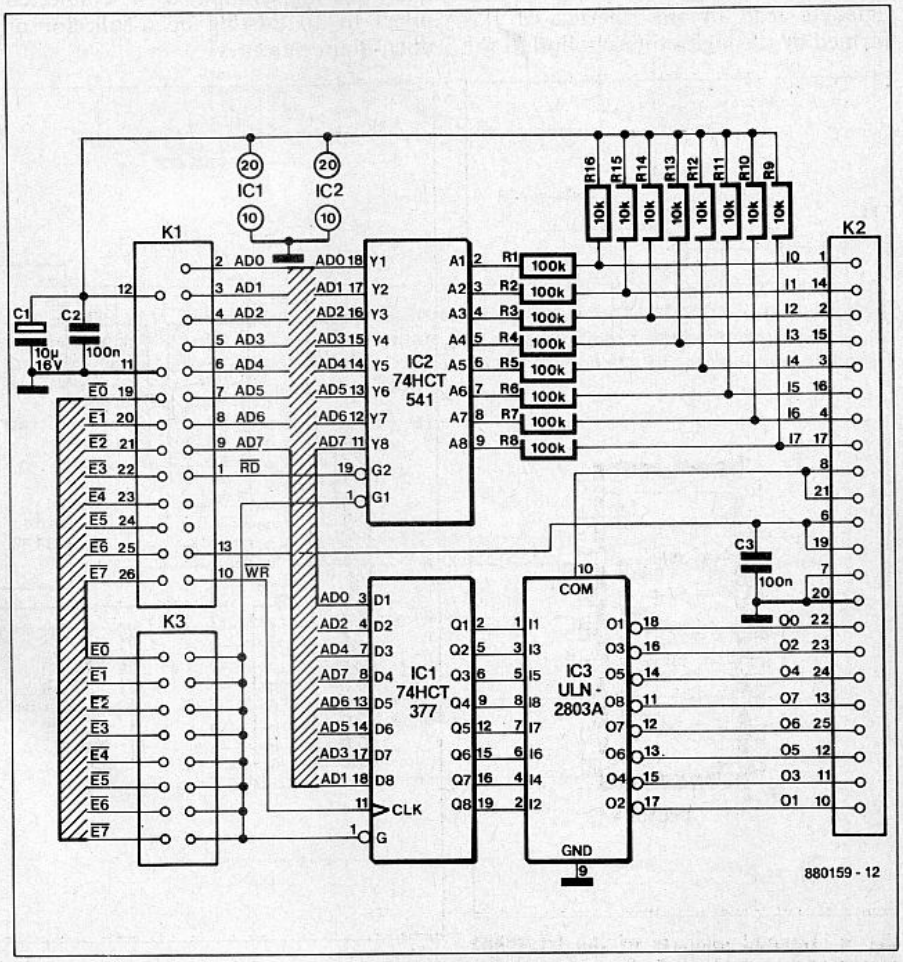


Fig. 3. Circuit diagram of the bidirectional digital interface. Up to 8 of these circuits can be controlled by a single address decoder.

(*short write* or *special write*), needed for controlling the D-A converter on the analogue output module.

Bidirectional digital input/output module

The circuit diagram of this basically simple unit is given in Fig. 3. Circuit IC_1 is an octal latch whose inputs are connected to the databus of the BASIC computer. Data is latched into IC_1 on the rising edge of the memory write signal, $\overline{WR}$, but only when input $\overline{G}$ is held logic low. This condition is satisfied when the address supplied by the computer falls within the range preset by the jumper on block K_3 (see Table 1.). When the processor writes a databyte to a digital output, e.g., at address $F600_H$, jumper E6 should be installed on K_3, and jumpers BD and AC on the address decoder board (Fig. 2).

Circuit IC_2 is controlled by the same enable line, $\overline{Ex}$, as IC_1, and in addition by the read signal, $\overline{RD}$, of the microcontroller. As a further configuration example, jumper $\overline{E4}$ should be installed on K_3, and jumpers BC and AD on the decoder board, to enable the microcontroller to read a databyte at address EC00 on the digital I/O board. The databyte read by the selected card is formed by the logic configuration of the signals applied to inputs I0 to I7 on the 25-way D connector, K_2. Note that the input lines have pull-up resistors, so that any non-connected input is read as a logic high level. The pull-up resistors allow the digital input to be connected direct to an existing open-collector or open-drain output.

Table 1. **Address assignment of I/O modules.**

Signal $\overline{Y7}$ defines address range E000 . . . FFFF, split in two by A11 and A12. Lines A8, A9 and A10 define 8 blocks of 256 addresses.

enable signal	wire links BD and AC	wire links BC and AD
$\overline{E0}$	F000 . . . F0FF	E800 . . . E8FF
$\overline{E1}$	F100 . . . F1FF	E900 . . . E9FF
$\overline{E2}$	F200 . . . F2FF	EA00 . . . EAFF
$\overline{E3}$	F300 . . . F3FF	EB00 . . . EBFF
$\overline{E4}$	F400 . . . F4FF	EC00 . . . ECFF
$\overline{E5}$	F500 . . . F5FF	ED00 . . . EDFF
$\overline{E6}$	F600 . . . F6FF	EE00 . . . EEFF
$\overline{E7}$	F700 . . . F7FF	EF00 . . . EFFF

All addresses in hexadecimal.

The Type ULN2803 in position IC_3 is an 8-way inverting power buffer composed of high-voltage, high-current darlington transistor arrays. This IC enables the digital output to directly control a wide range of loads, such as relays, solenoids, stepper motors and LED displays. Figures 4a and 4b show the inter-

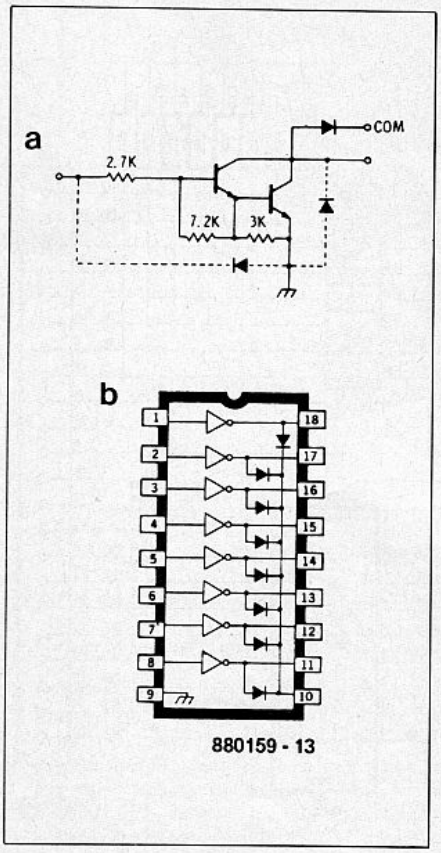


Fig. 4. Internal diagram of the ULN2803 from Sprague. Each of the 8 surge-protected darlington transistors in this chip can switch (inductive) loads of up to 500 mA.

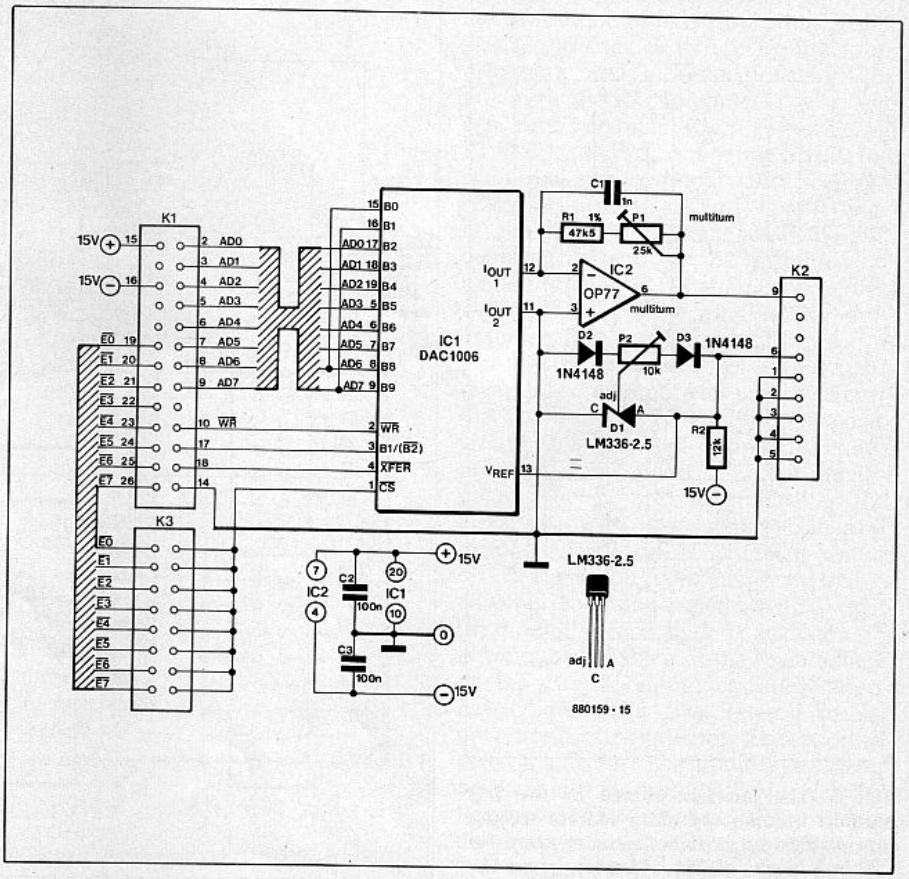


Fig. 5. The analogue output module is based around a 10-bit digital-to-analogue converter Type DAC1006 from National Semiconductor. The output voltage span is from 0 to 10.23 V in 10 mV steps.

nal structure of the ULN2803. Note that the buffers are of the inverting type, and that internal anti-surge diodes are provided to prevent damage to the open-collector output transistor when the current through the inductive load (relay coil) is interrupted. The anti-surge diodes are internally connected to a common rail, which is brought out to pin 10. This means that the supply voltage for the inductive loads controlled by the ULN2803 can be connected to pins 21 and 8 of K_2.

Analogue output module

The heart of the D-A module shown in Fig. 5 is formed by IC_1, a Type DAC1006. This 10-bit DAC is remarkable for its excellent stability and capability to be controlled from an 8-bit bus. Loading of data (0 to 1023_{10}) is done in two successive operations, under control of the logic level of the BS (byte select) signal applied to pin 3. This signal comes direct from the microcontroller 8052AH-BASIC via an output line of port P1. Users should decide for themselves which of these lines is to be used for providing signal BS.

The Type DAC1006 has a few pecularities which call for a rather special circuit configuration around it. Firstly, the DAC has a specific requirement as regards the duration of the databyte. The timing diagrams of Fig. 6 show that databytes are present on the bus for only 40 µs after the $\overline{WR}$ pulse (Fig. 6a). The DAC1006, however, requires data to be present for at least 200 ns (Fig. 6b). This problem is solved by monostable IC_2 in the address decoder circuit (Fig. 2). Note that the 74LS122 used for this purpose is not available in the HCT version.

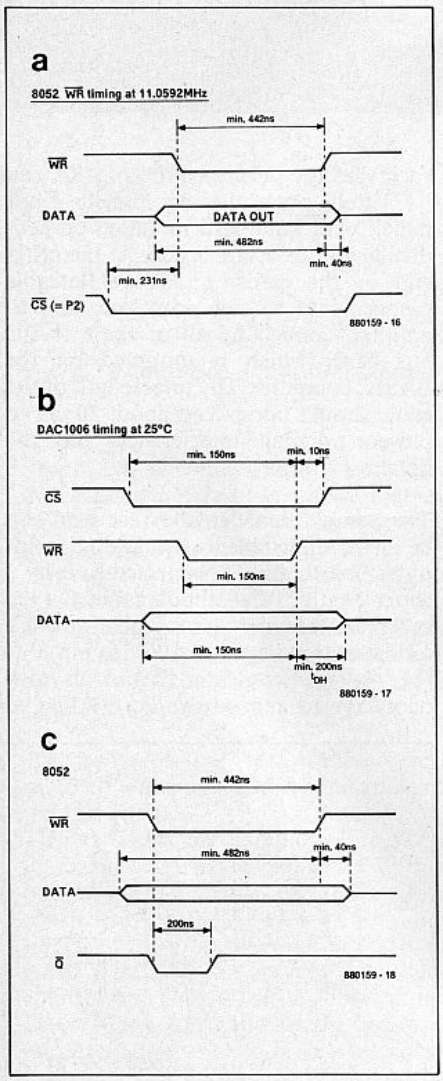


Fig. 6. For the DAC1006 to operate corectly, data should remain stable on the the databus for at least 200 ns following the rising edge of the $\overline{WR}$ pulse (Fig. 6b), which is not so on the databus of the 8052AH-BASIC (Fig. 6a; f_{CL}=11.0592 MHz). A monostable multivibrator is, therefore, required to shorten the $\overline{WR}$ pulse (Fig. 6c).

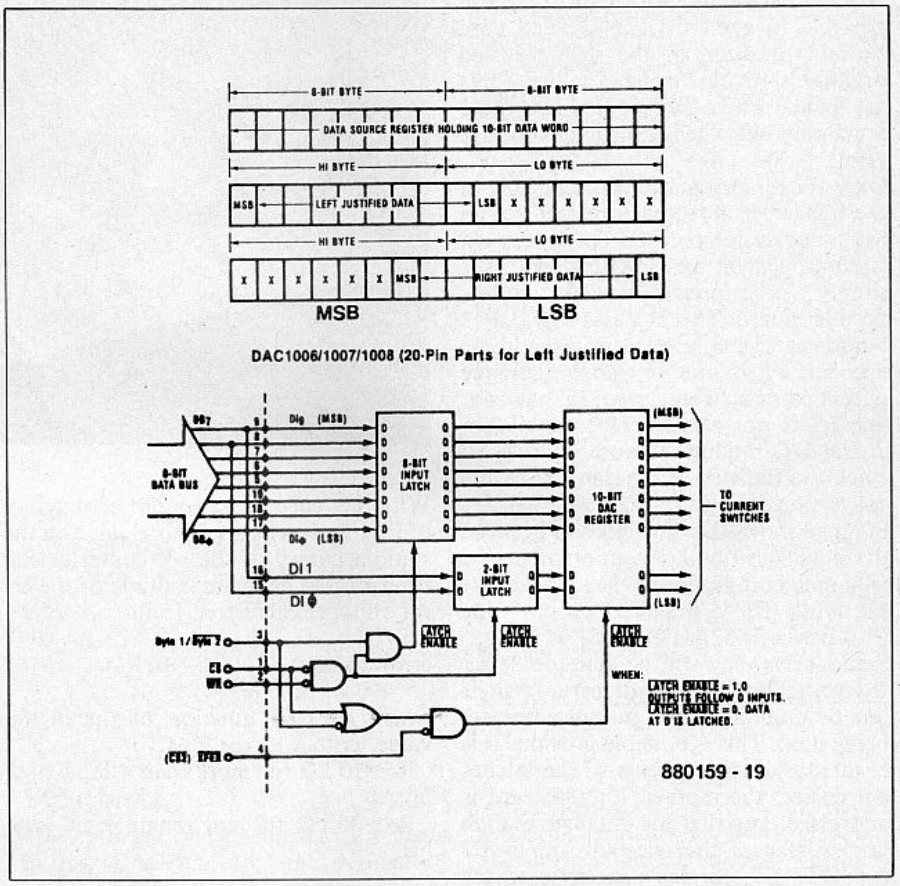


Fig. 7. The DAC1006 expects 10-bit, right-justified, data in a 16-bit dataword. Signal BS, together with $\overline{WR}$ and $\overline{CS}$, is needed to ensure that data from the 8-bit databus is sequentially latched into the device. A further signal, XFER, effects the transfer of the complete dataword from the latches to the internal conversion register.

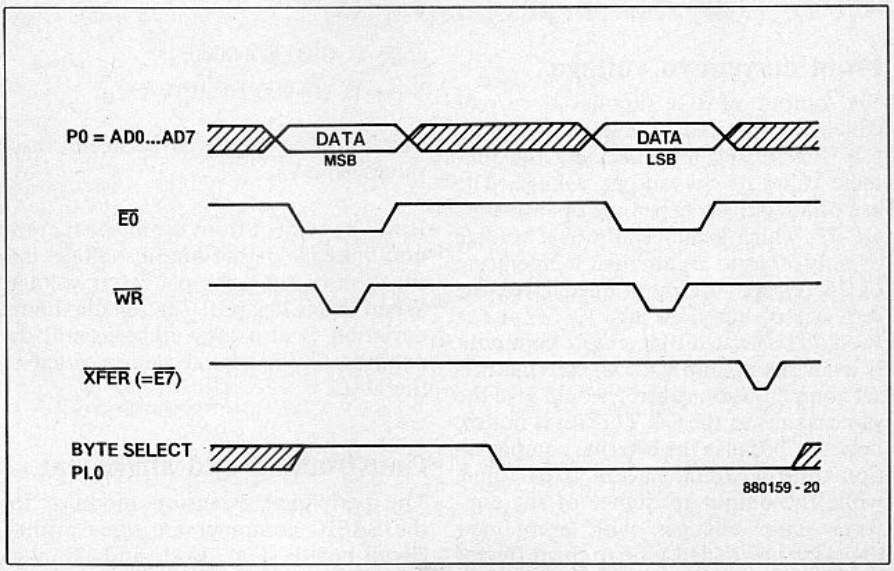


Fig. 8. Timing diagram relevant to the loading of data in the D-A converter.

Loading the DAC

The second peculiarity of the Type DAC1006 has to do with the way it is loaded with digital data. Figure 7 shows how signal BS allows the chip to latch the 10-bit dataword as 8, followed by 2, bits. Unconventionally, the 10 databits are left-justified in 16 available bit locations. Fortunately, in spite of the slightly unusual configuration of lines AD0 to AD7, and B0 to B9, it is still possible to achieve right-justified data by multiplication of the right-justified original 10-bit data by 64. The first 8 bits are loaded when BS is logic high, the 2 remaining bits when BS is logic low (see also Fig. 8).

Once the 10-bit dataword is available in the latches, it is ready to be transferred to the conversion register. This operation is controlled by signal XFER, which is simply $\overline{Ex}$ supplied by the address decoder board. This explains why only 7 boards can be connected to the address decoder when one or more analogue output cards are being used. In that case, line $\overline{E7}$ is not available for enabling a digital I/O module because it serves to clock the transfer of the databits to the conversion register in the DAC1006.

Figure 8 shows the time relation between the signals involved. As an example, the analogue output module is addressed by $\overline{E0}$, while BS is provided by port line P1.0 of the 8052AH-BASIC.

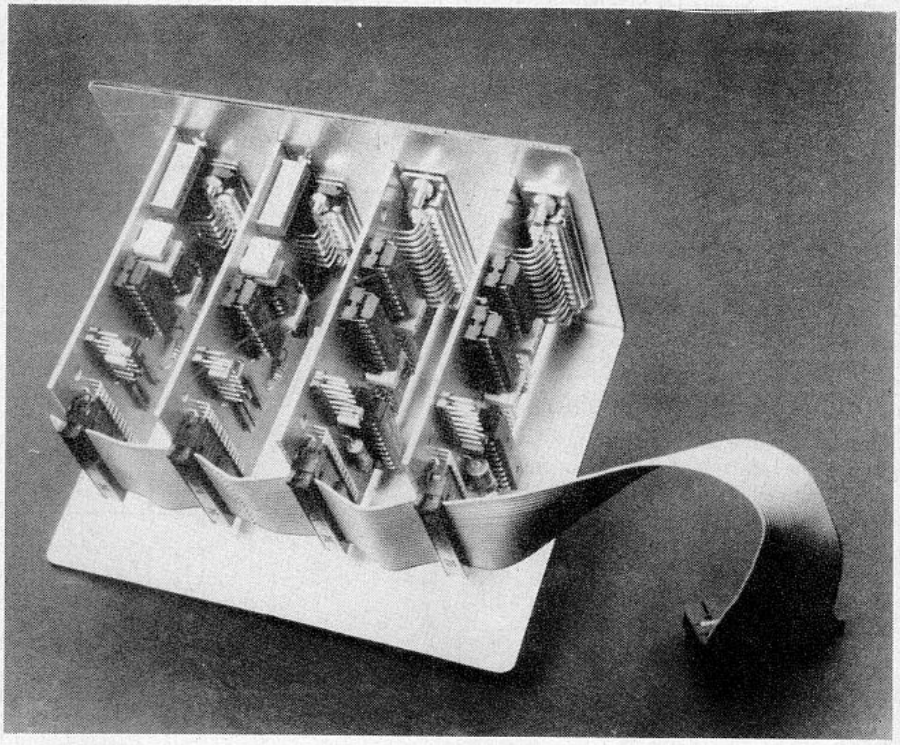
Smart users may still be able to use $\overline{E7}$ for addressing an eighth card, even if one or more analogue output cards are being used. This is possible provided it is ensured that the contents of the latches are correct the moment the 8th card is addressed, **and** that the databyte written in the latch of the selected card by $\overline{E7}$ (= XFER) is correct also (refer to the listing in Table 2).

The external reference voltage for the DAC1006 is provided by D_1, whose thermal coefficient can be accurately compensated by preset P_2.

From current to voltage

The output of IC_1 supplies a current which is converted to voltage in opamp IC_2. Preset P_1 allows defining the full-scale value of the output voltage. The use of a relatively expensive opamp Type OP-77, which achieves an offset voltage of only 50 μs at an ambient temperature of 25° C, may be questioned given the step size of 'only' 10 mV.

It could be argued that a more commonly available opamp with an external offset compensation resistor would give the same results as the OP-77. This is not so, however, because the external compensation resistor would have a fixed value, while the output resistance of the converter chip changes with every new digital value loaded, due to the different configuration of the internal R-2R ladder network.



With reference to the simplified diagram of Fig. 9, the effect of this change on the static accuracy of the I-V converter can be expressed as the magnitude of the error voltage, calculated from

$$\text{error voltage} = V_{os}(1+R_F/R_O)$$

where R_O is a function of the digital value written to the DAC:

$R_O \approx 10$ kΩ for more than 4 logic high bits;

$R_O \approx 30$ kΩ for any single logic high bit.

Therefore, the offset gain varies as follows:

code = 001111111111:

$V_{err1} = V_{os}(1+10^4/10^4) = 2V_{os}$.

code = 010000000000:

$V_{err2} = V_{os}(1+10^4/3\times10^4) = 4/3 V_{os}$.

The error difference between these values is $2/3 V_{os}$.

It will be evident from the above that the non-linearity of the output voltage is a function of the opamp's offset voltage. When this is low (OP-77), the maximum deviation is also low, athough still dependent of the digital value written to the DAC.

Construction and alignment

The peripheral extension modules for the BASIC computer are three printed circuit boards (Figs. 10, 11 and 12) interconnected by a bus formed by flat ribbon cable. The layout of the boards is such that the output connector, K_2, can be fitted onto the equipment front panel, with the board mounted perpendicular to this at the inside. At the other end of the cards, a 26-way flatcable plugged into K_1 runs from one card to another, connecting all of these to the bus card, which is mounted on the BASIC computer. The total length of the cable should not exceed about 30 cm to prevent digital interference on the databus.

The address decoder/interface card can be fitted direct on to the BASIC computer board, and is connected to it by a short length of flat ribbon cable. On the computer board, connect pin 7 of IC_3 (address decoding signal $\overline{Y7}$) to pin 8 of the 40-way connector (K_2). It is also necessary to choose the Port 1 line to

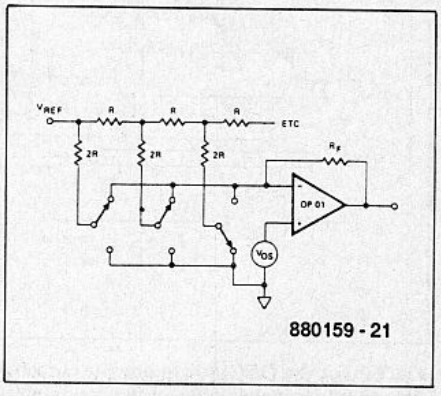
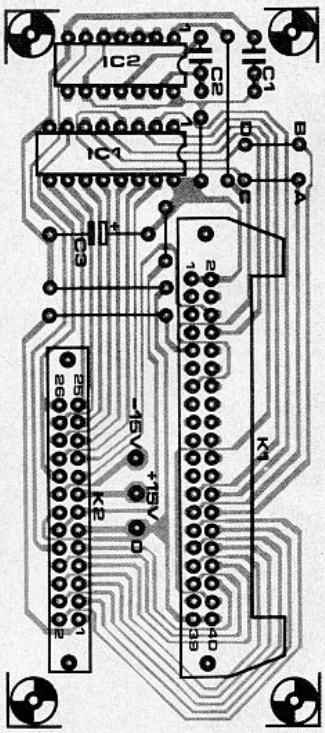


Fig. 9. Variation in output resistance of the DAC as a function of the converted code gives rise to a variable offset current at the input of the opamp, which translates current to voltage, and so magnifies the offset voltage. Obviously, the offset voltage of the opamp itself should be as low as possible.



Parts list
ADDRESS DECODER BOARD

Capacitors:
C_1 = 100n
C_2 = 22p
C_3 = 10µ; 10 V

Semiconductors:
IC_1 = 74HCT138
IC_2 = 74LS122

Miscellaneous:
K_1 = double-row 40-way right-angled header, or 40-way right-angled male header with eject handles.
K_2 = double-row 26-way straight PCB header.
PCB Type 880159

Fig. 10. Printed circuit board for the address decoder.

supply BS. The connection between pin 6 of K_2 and pin 19 of K_1 shows that we have opted for Port 1 line P1. Any other line is equally suitable, as long as the software for the I/O modules takes this into account.
If it is decided not to use the analogue output module, the last mentioned link can be omitted. Similarly, the ±15 V supply is not required then.

The modules are ready after being assigned a memory address by placing a jumper on K_3.
There are only two, simple, adjustments to carry out on the analogue output board(s). First, correct the temperature coefficient of the LM336-2V5 by adjusting P_2 for a reference voltage of 2.490 V measured at pin 6 of the output connector, K_2. Next, write 1000_{10} to the DAC (10 mV/LSB) and set the full-scale output voltage to 10.00 V with the aid of P_1.

The I/O modules discussed have a relatively low current consumption, and are, therefore, conveniently powered from the existing supply for the BASIC computer. The analogue board draws about 10 mA, the digital board and the decoder each about 20 mA.

Final notes

The contents of the conversion register in the DAC1006 are not defined at power-on, so that the output voltage may not be nought then. When an XFER pulse is received by a DAC, all other DACs connected respond to this simultaneously. This means that the contents of the latches should correspond to the desired output voltage, which may not be the case at power-on.
The analogue and digital ground lines may only be connected on the address decoder board.

Table 2. Examples of elementary command routines

For analogue module:

```
100   E0 = 0F000H              REM output address (see K3)
110   XF = 0F700H              REM dummy address (transfer)
120    INPUT X                 REM get byte to convert
130   X = X * 64               REM justify left
140   PORT1 = 1                REM write byte
150   XBY(E0) = X/256          REM i.e. MSB, and then
160   PORT1 = 0                REM LSB
170   XBY(E0) = X.AND.0FFH     REM (only bits 6 et 7 are useful)
180 XBY(XF) = 0                REM clock 10-bit transfer
190 GOTO 120                   REM end of loop
```

For digital module:

```
10 E1 = 0F100H        REM module address (see K3)
20 Y = XBY(E1)        REM read input byte from Y
30 XBY(E1) = 00F3H    REM write byte F3
```

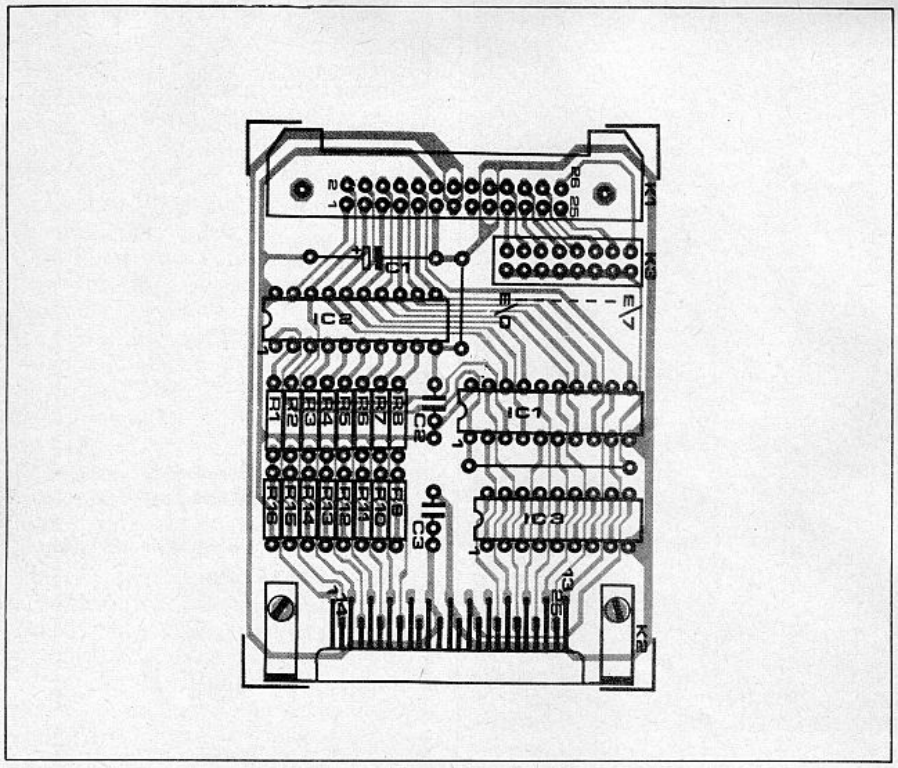


Fig. 11. Printed circuit board for the digital I/O module.

Parts list
DIGITAL I/O BOARD

Resistors:
R1 . . . R8 incl. = 100K
R9 . . . R16 incl. = 10K

Capacitors:
C1 = 10µ; 16 V
C2;C3 = 100n

Semiconductors:
IC1 = 74HCT377
IC2 = 74HCT541
IC3 = ULN2803A

Miscellaneous:
K1 = double-row 26-way right-angled header, or 26-way right-angled male header with eject handles.
K2 = 25-way D connector, male, with right-angled pins.
K3 = double-row 16-way straight PCB header.
1 jumper for mounting on K3.
PCB Type 880163

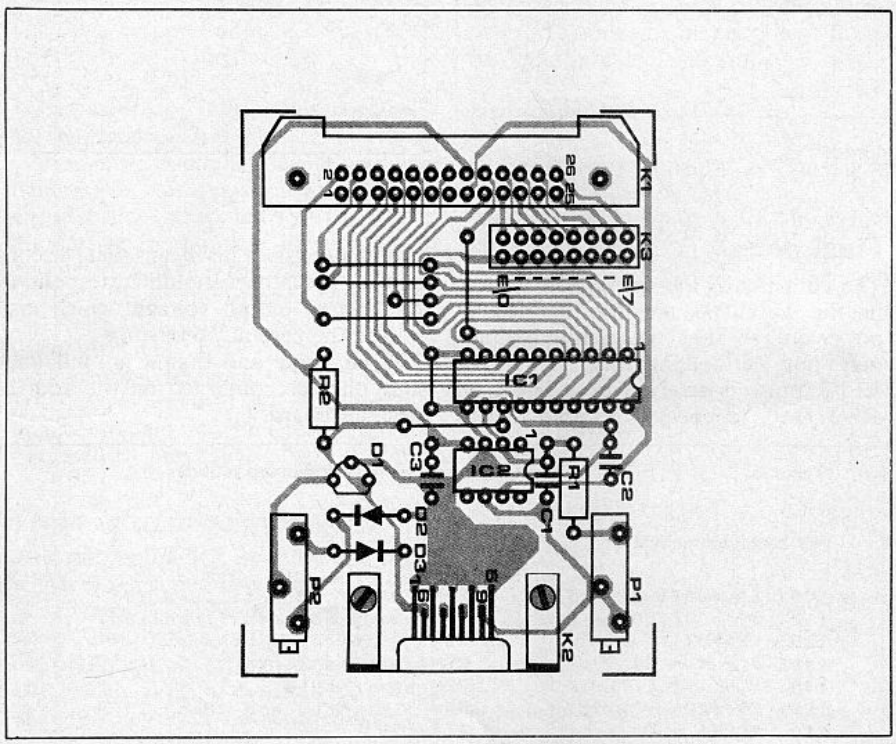


Fig. 12. Printed circuit board for the analogue output module.

When the logic outputs are used only for driving other digital circuits, the ULN2803 need not be fitted, and wire links may be installed between the PCB connections intended for the inputs and outputs of the chip.
Finally, do not forget that $\overline{E7}$ can not normally be used as a board selection signal because it is needed as XFER shared by the analogue output modules.

Parts list
ANALOGUE OUTPUT BOARD

Resistors:
R1 = 47K5 1%
R2 = 12K
P1 = 25K or 22K multiturn preset
P2 = 10K multiturn preset

Capacitors:
C1 = 1n0
C2;C3 = 100n

Semiconductors:
D1 = LM336-2V5
D2;D3 = 1N4148
IC1 = DAC1006 (National Semiconductor)
IC2 = OP-77 (PMI)

Miscellaneous:
K1 = double-row 26-way right-angled header, or 26-way right-angled male header with eject handles.
K2 = 9-way D connector, male, with right-angled pins.
K3 = double-row 16-way straight PCB header.
1 jumper for mounting on K3.
PCB Type 880162

PREAMPLIFIER FOR PURISTS

The ideal preamplifier is a short piece of wire. Unfortunately, we have not reached that state yet. A practical preamplifier must match signal levels and impedances of the various units in the system. None the less, the preamplifier presented here approaches the ideal state: the electronics in the signal path have been kept to a minimum.

Technical Specification

Signal-to-noise ratio	> 110 dB
Harmonic distortion	f = 1 kHz: < 0.01%
	f = 10 kHz < 0.01%
Channel separation	tuner:
	f = 1 kHz ≅ 95 dB
	f = 10 kHz ≅ 75 dB
	f = 20 kHz ≅ 70 dB
	CD:
	f = 1 kHz ≅ 85 dB
	f = 10 kHz ≅ 65 dB
	f = 20 kHz ≅ 60 dB
For all measurements:	U_o = 1 V
	all used outputs terminated in 10 kΩ
	all unused outputs terminated in 600 Ω

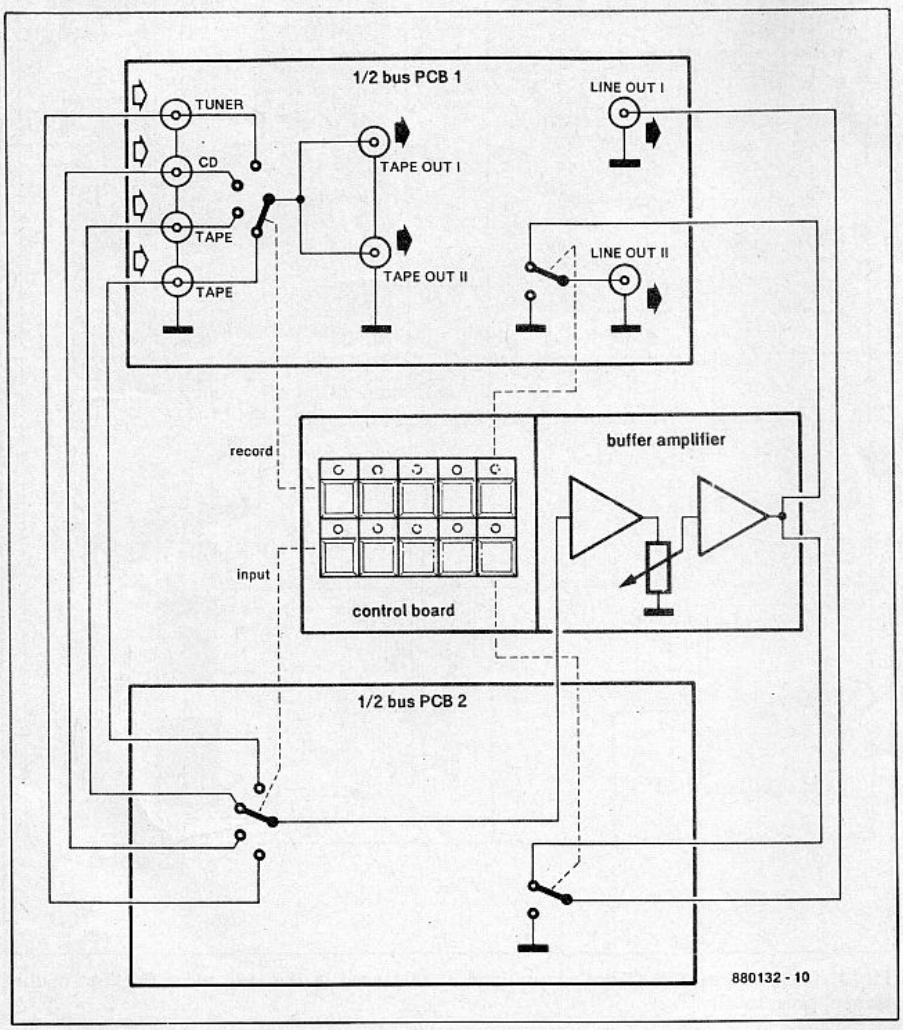


Fig. 1. Block schematic of the preamplifier.

Since the advent of the compact disc player, more and more music lovers have added one to their hi-fi system. In fact, the stage has now been reached where a great many hi-fi enthusiasts no longer, or hardly ever, use their conventional record player. The present preamplifier is aimed at these listeners. Their hi-fi system will normally consist of a CD player, a digital audio tape (DAT) player, a reel-to-reel tape recorder, a tuner, and a power amplifier.

The block diagram in Fig. 1 shows the layout of the preamplifier. The control board contains 10 switches, each of which controls a high-quality relay. The relays select the various inputs and outputs. In addition, independent input selection is possible for the two tape outputs and the line output. This makes it possible to record from one signal source and at the same time to listen to another one via the loudspeakers.

The two bus boards are adaptations of that used for the 'Top-of-the-Range Preamplifier' [1].

It is one of the tasks of a preamplifier to match the input and output impedances of the various units in the audio system. Another one is volume control. These requirements are met by the buffer-amplifier, the only active element in the signal path.

Bus boards

Input and output sockets, relays and associated components are housed on the same board as used in Ref. 1 — see Fig. 3. The shaded areas indicate the changes made for the present design: the components in these areas are not used.

Bus board 1 contains the input and output sockets, the potential dividers that equalize the input signal levels, and the input selectors for the tape outputs. These selectors, controlled from the control board, operate four high-quality relays, ReA to ReD incl.. The relays determine which input signal is passed to the two tape output sockets.

The board also houses the independently switched output sockets. Line output 1 is controlled by relay ReF on bus board 2, and line output 2 by relay Ref on bus board 1. This arrangement does not con-

Fig. 2. Prototype of the preamplifier.

tradict the design criterion of using the shortest possible path, because the two boards are sandwiched in the construction phase.

Buffer-amplifier

Apart from possessing the highest possible audio qualities, the amplifier must (a) present a minimal load to the input circuit; (b) be equipped with a volume and balance control; and (c) have a low output impedance. Its circuit diagram is shown in Fig. 4. The difference between it and most other amplifiers of this nature lies in the choice of components. More particularly, the type of opamp is important. The one used here can not easily be bettered. Further, the use of 1% resistors is not intended to achieve high accuracy, but rather to ensure long-term stability.

Only one capacitor is used in the signal path, and it is, of course, of the highest quality for audio purposes. No capacitors are used in the output of the amplifier, since the inputs of the power amplifier are normally fitted with one. In any case, the off-set voltage of the second stage is so low that even where a DC-coupled power amplifier is used no direct-voltage problems will ensue.

The purpose of resistors R_{32}, R_{33}, R_{40} and R_{41} is mainly to decouple the two outputs from one another. They are also of benefit where long connections or capacitive loads occur. In most cases they may be omitted (replaced by wire links). This is particularly so if only one output is used.

The balance control is arranged as two independent potentiometers, one for each channel. This arrangement has the advantage that not only the balance but also the output level may be set in accordance with the input sensitivity of the power amplifier.

Control board

The relays are controlled electronically. This has the disadvantage that after switch-off the amplifier no longer 'remembers' which input source was

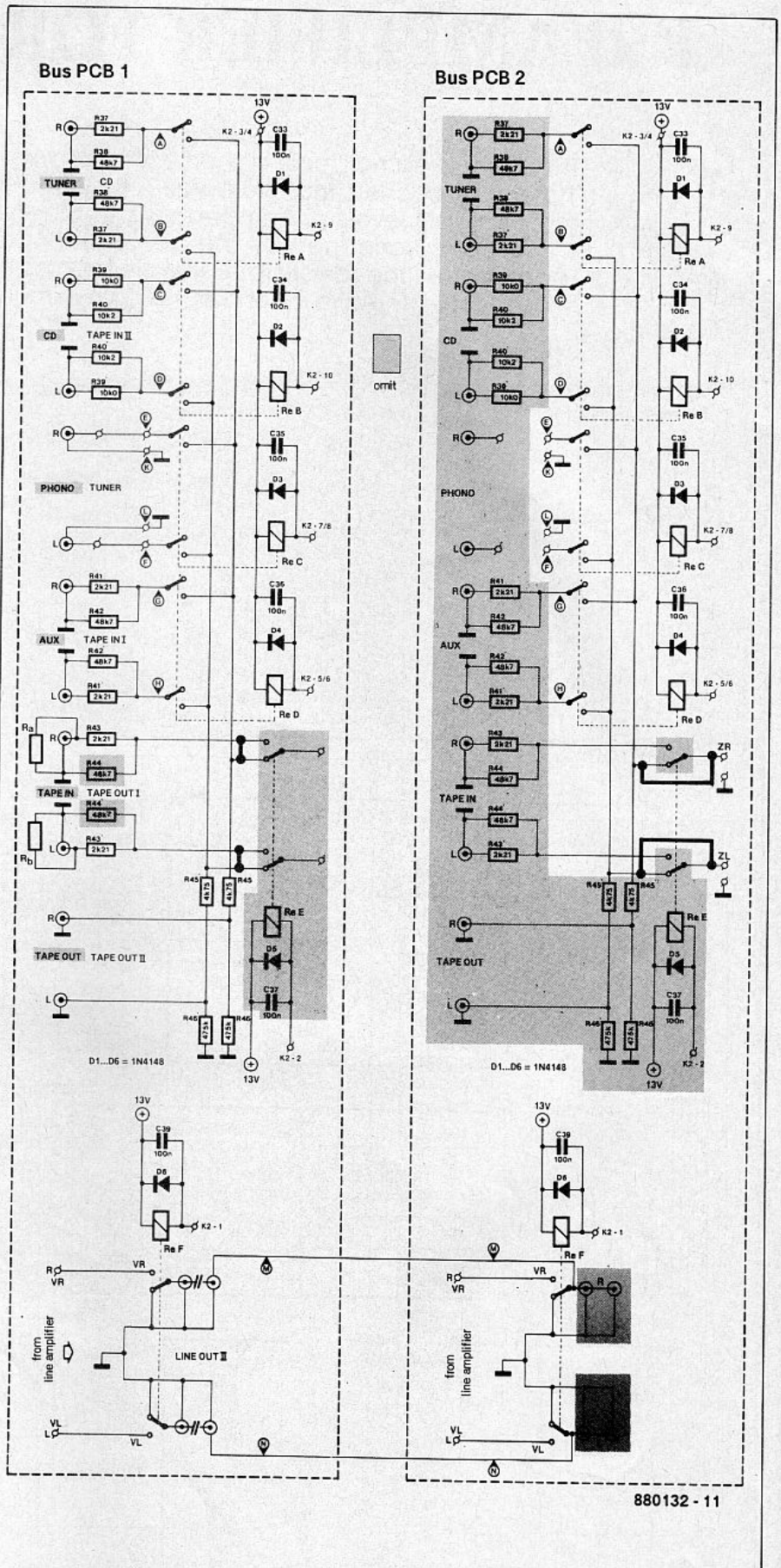


Fig. 3. The two bus boards are adaptations of that used in the very succesful 'Top-of-the-Range' preamplifier.[1]

(1) Shaded components are not used.

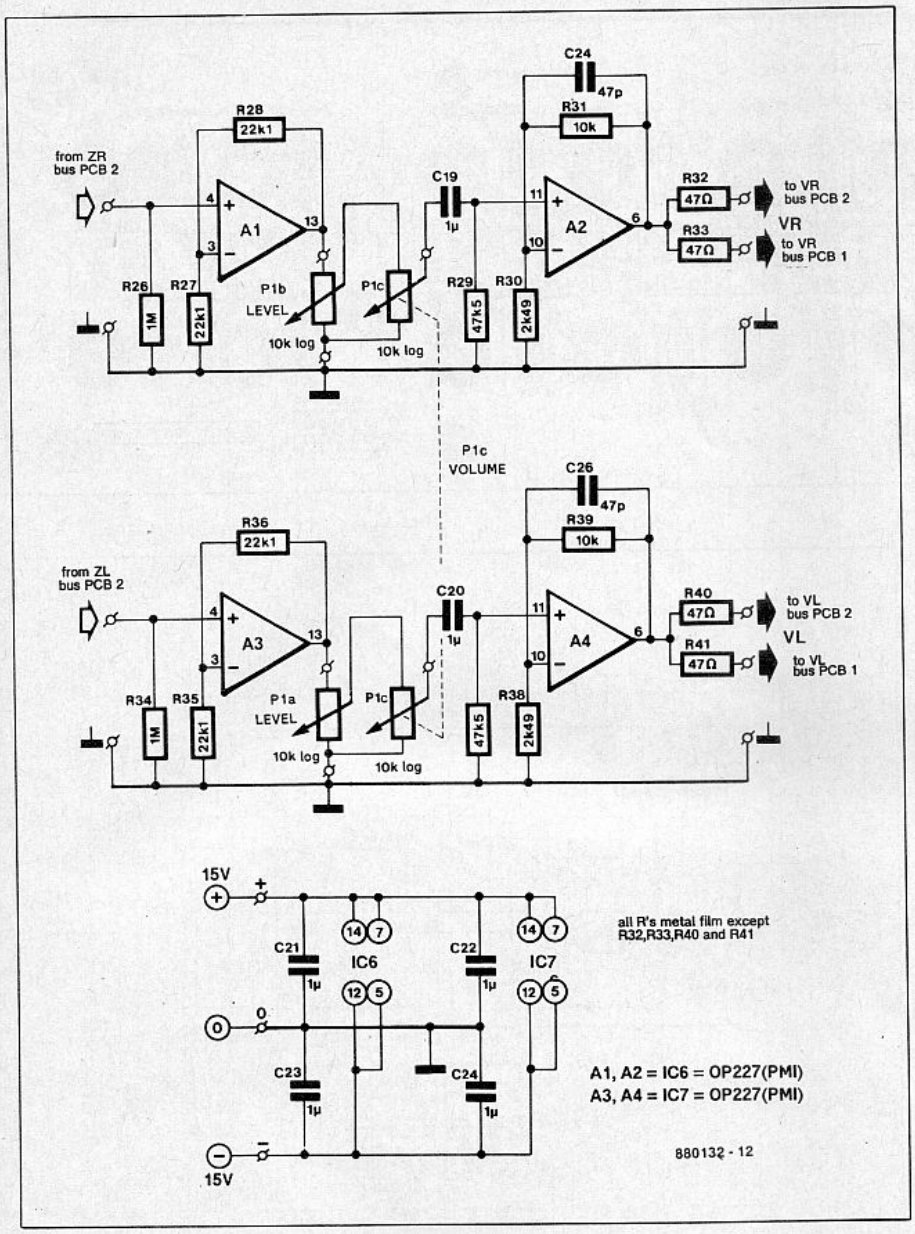


Fig. 4. Circuit diagram of the buffer-amplifier.

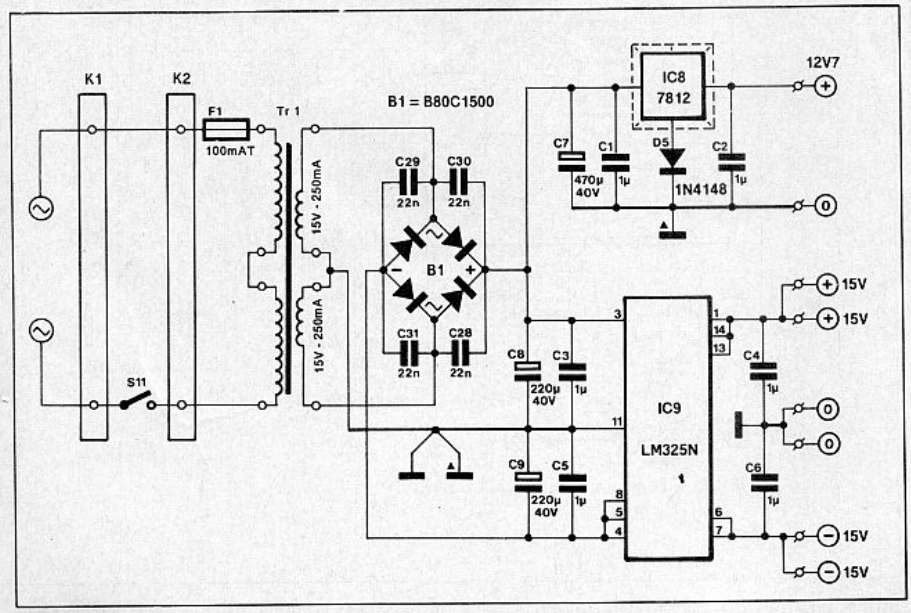


Fig. 5. Circuit diagram of the power supply.

selected, but the advantage that you don't get blown out of your seat when on subsequent switch-on the tuner is tuned to a hard-rock programme and the volume is set fairly high.

The control-circuit is so arranged that after switch-on no input source is selected and that the user may select no, one, or two outputs.

The control circuit may be divided into three parts: (a) one for the control of the output relays; (b) one for the control of the recording source relays; and (c) one for the control of the input source relays.

The circuit of (a) is given in Fig. 7a. It is based on bistables FF_1 and FF_2, which store the selected setting. Since the $\overline{Q}$ output of FF_2 is connected to the D output, each clock pulse (generated when either S_1 or S_2 is pressed) will toggle the relevant bistable. In this way, a selected output is switched off and a switched-off one is selected.

To ensure smooth operation of the circuit, the switches are connected to the clock input of the bistables via debounce circuits N_1-N_2 and N_3-N_4.

The two circuits are intercoupled with the aid of diodes D_1 to D_4 incl. and resistors R_{10} and R_{11} in a manner that makes the interdependence between the relays comparable to that of mechanically coupled switches. This makes it impossible for two relays to be actuated simultaneously.

Note that the diode-resistance logic is formed only by the relevant resistor, R_{10} or R_{11}, and the diode that is connected to the bistable, D_2 or D_4 as the case may be. The other diode, D_1 or D_3, only serves to prevent the output of the bistable being shorted to ground by the associated switch.

Diode D_2 and R_{10}, and D_4 and R_{11}, form and NAND gate. The output of that gate, i.e., the junction of the diode and resistor, is 0 only if the associated circuit output is selected and the switch of the other channel is operated. This ensures that when an output is selected, the other output is switched off. In spite of this arrangement, it is possible to switch on both outputs simultaneously. To achieve this, the sequence in which the switches need to be operated is important. It is necessary for the switch associated with the switched-off output to be depressed first and to be held down while the other switch is pressed. If this sequence is reversed, the outputs are changed over. If both outputs are switched off, it is permissible for both switches to be pressed simultaneously.

To ensure that the bistables are in a given state on switch-on, their set and reset inputs are provided with RC networks. If either C_{11} or C_{13} is replaced by a wire link, the associated output remains off. If the capacitors are fitted as shown, the bistable output will be 'on' about a second after switch-on.

Because of the relative large time-

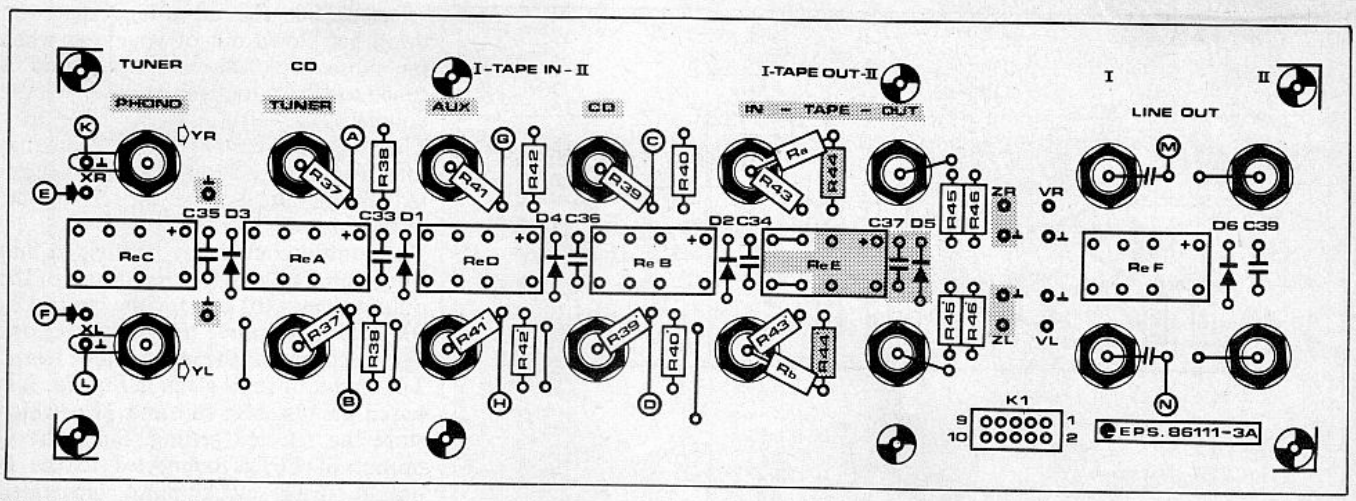


Fig. 6. Component layout of bus board 1.(1)

Parts list

BUSBOARD 1

Resistors (± 1%; metal film):
R37;R37' = 10K0
R38;R38' = 10K2
R39;R39';R41;R41' = 2K21
R40;R40';R42;R42' = 48K7
R43;R43';R45;R45' = 4K75
R46;R46';Ra;Rb = 475K

Capacitors:
C33..C36 incl.;C39 = 100n

Semiconductors:
D1...D4 incl.;D6 = 1N4148

Miscellaneous:
REA...RED incl.;REF = DS2E-M-DC12V (manufacturer: SDS), or W11V23102-A006-A111 (manufacturer: Siemens), or M1-12 or M1B12H (manufacturer: Meisei), or G2V-2 (manufacturer: Omron).
16 off gold-plated phono sockets, e.g. Type T-710G (Monacor).
10-way male PCB header.
PCB Type 86111-3a

constant R_5-C_{10}, the selected outputs will not be able to react to S_1 or S_2 for a couple of seconds (i.e., the duration of the set pulse).

The second and third sections of the control board consist of identical circuits — see Fig. 7b.

Circuit IC_5 is an eight-fold inverter-driver that prompts the actual control circuits around IC_3 and IC_4 to provide the input relays and indicator LEDs with adequate current.

The drivers are controlled by two BCD-to-decimal decoders, IC_1 and IC_4, which are arranged in a manner to make it impossible for either IC to switch on more than one input at a time. If more than one switch is pressed at the same time,

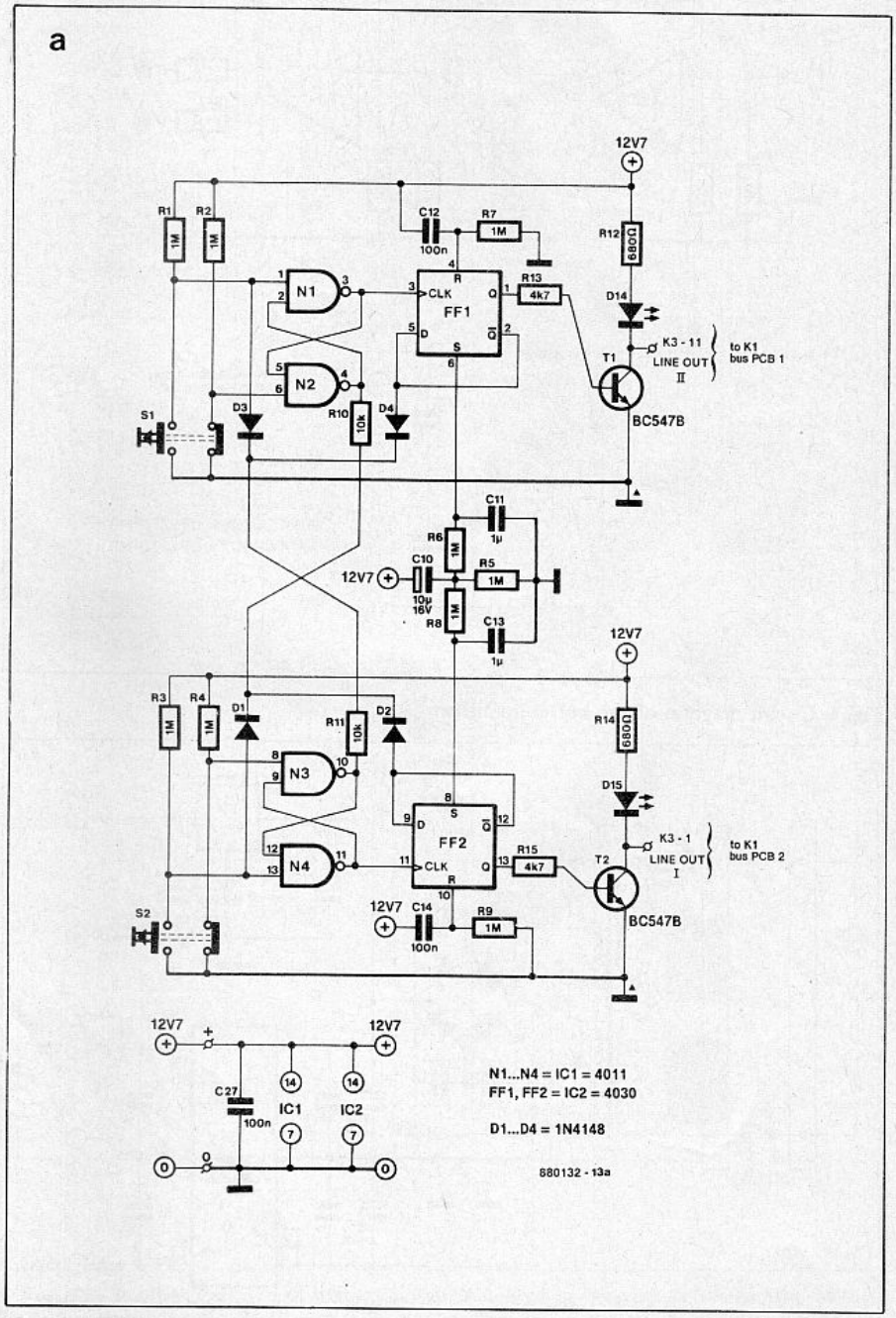


Fig. 7. Circuit diagram of the control section with the output switches in (a), and the switches for input source and recording in (b).

(1) Shaded Components not used

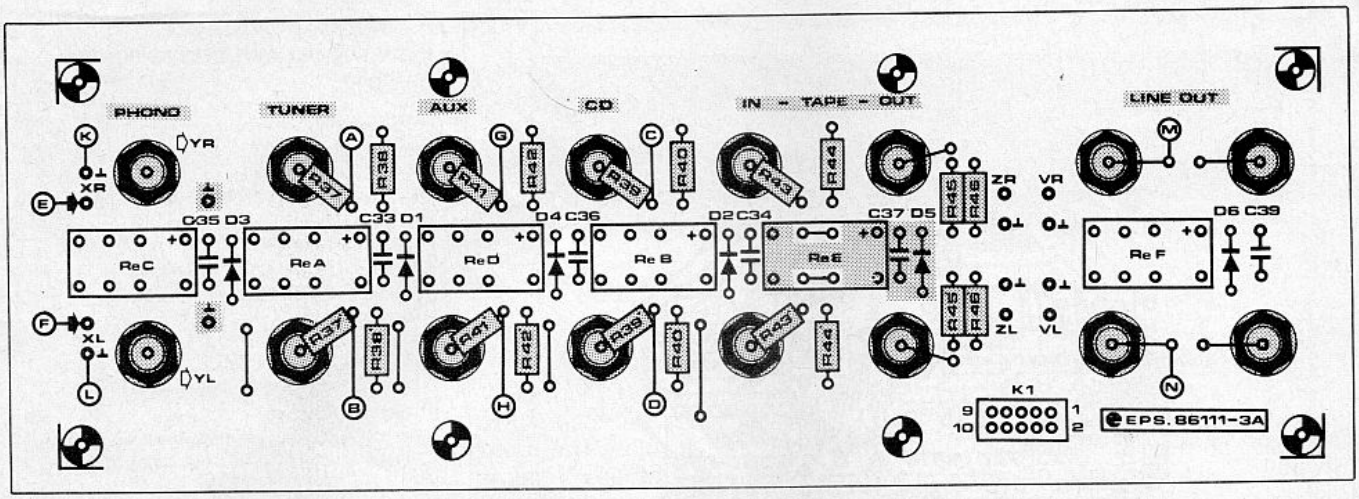
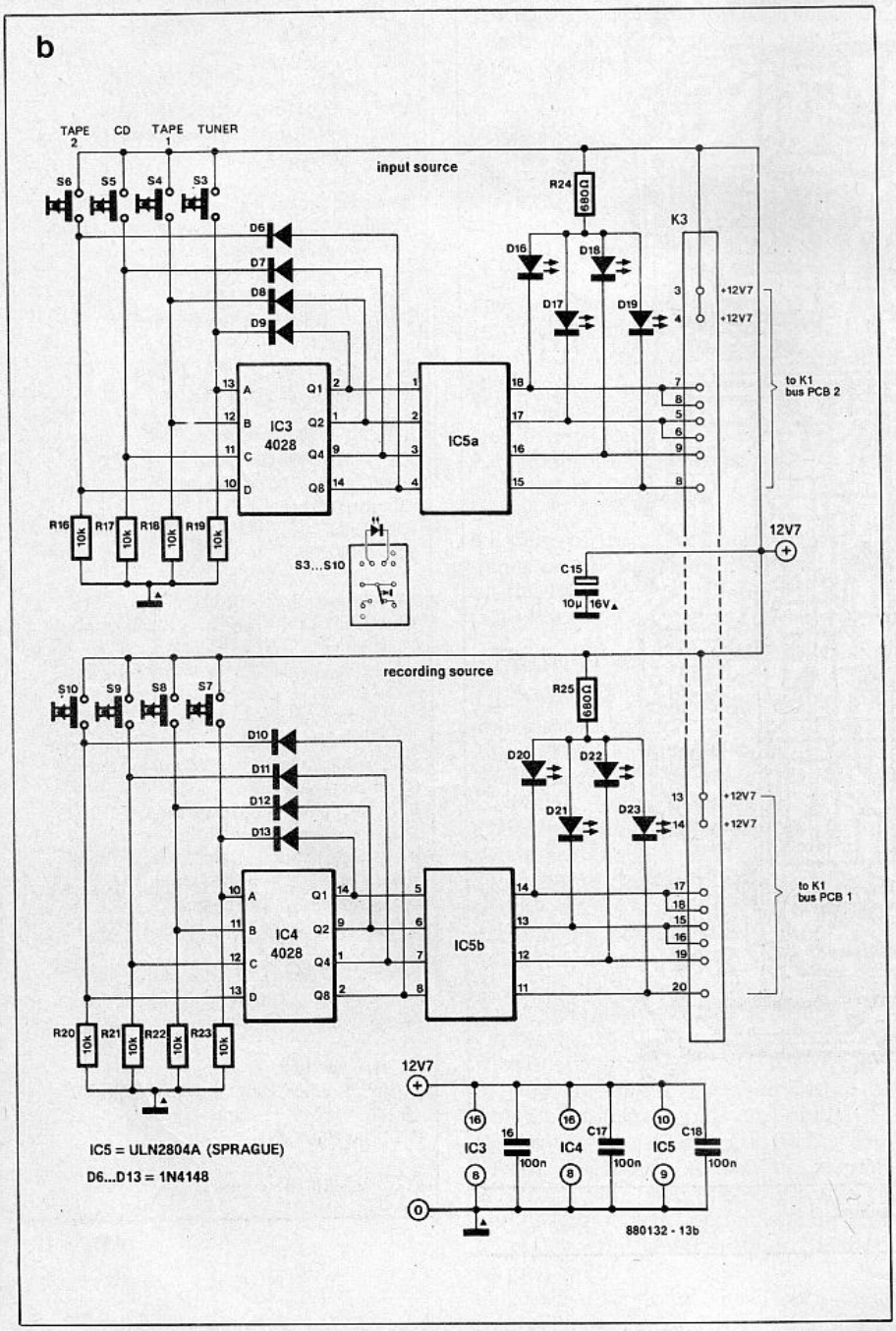


Fig. 8. Component layout of bus board 2.[1]



Parts list

BUSBOARD 2

Capacitors:
C33...C36 incl.;C39 = 100n

Semiconductors:
D1...D4 incl.;D6 = 1N4148

Miscellaneous:
ReA...ReD incl.;ReF = DS2E-M-DC12V (manufacturer: SDS), or W11V23102-A006-A111 (manufacturer: Siemens), or M1-12 or M1B12H (manufacturer: Meisei), or G2V-2 (manufacturer: Omron).
K1 = 10-way male PCB header.
PCB Type 86111-3a

no input is selected at all. This is achieved by the use of BCD codes of which only one bit is high: those for 1, 2, 4, and 8. These codes are generated when only one switch is pressed. The hold function is obtained by feedback of the relevant output via a diode. As soon as an output is high, it causes a code at the input which ensures that the output remains high. This state can be altered only by operating another switch: the decoder then changes over.

During the change-over (which lasts for a few hundred nanoseconds), or if more than one switched is pressed (which may last longer), none of the input relays can be energized. If more than one switch is pressed at the same time, the decoder will be presented with several high bits. One of the six not-connected decoder outputs will then go high and all connected outputs will become low.

(1) Shaded Components not used

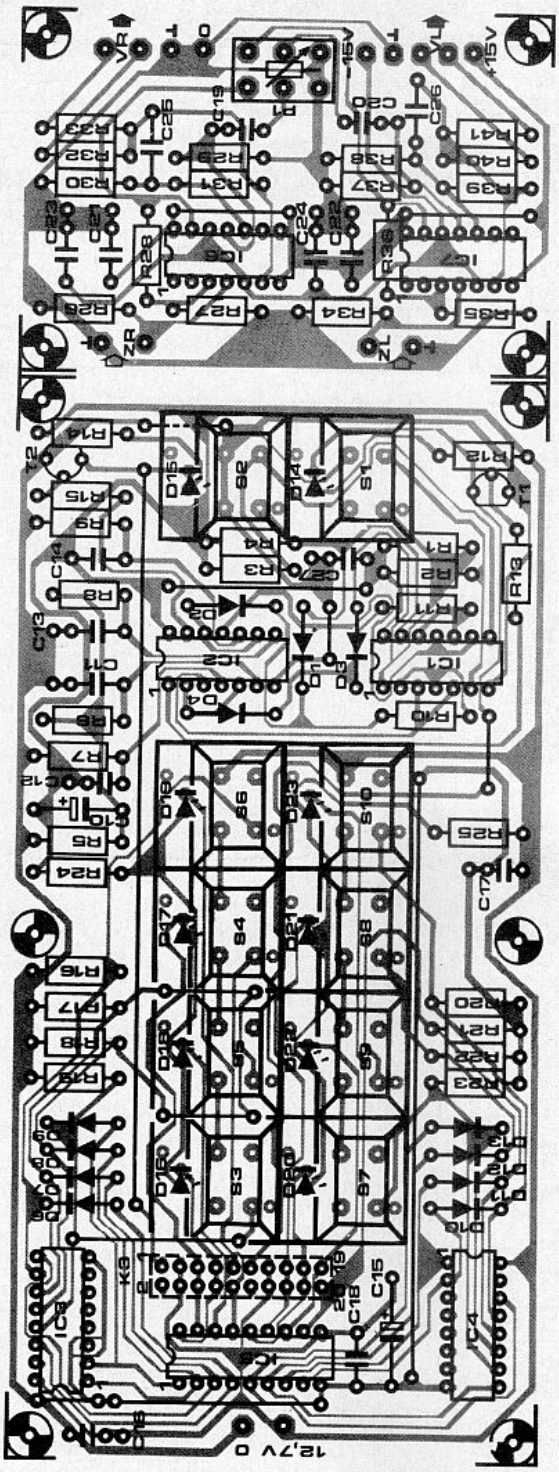


Fig. 9. Component layout of the power supply board.

CONTROL, LINE AMPLIFIER AND POWER SUPPLY

Resistors:
R1 . . . R9 incl. = 1M0
R10;R11;R16 . . . R23 incl. = 10K
R12;R14;R24;R25 = 680R
R13;R15 = 4K7
R26;R34 = 1M0; 1%
R27;R28;R35;R36 = 22K1; 1%
R29;R37 = 47K5; 1%
R30;R38 = 2K49; 1%
R31;R39 = 10K; 1%
R32;R33;R40;R41 = 47R
P1a;P1b = 10K logarithmic potentiometer (Bourns, Spectrol)
P1c = 10K stereo logarithmic potentiometer (Alps)

Capacitors:
C1 . . . C6 incl.;C11;C13;C19 . . . C24 incl. = 1μ0; MKT
C7 = 470μ; 40 V
C8;C9 = 220μ; 40 V
C10;C15 = 10μ; 16 V
C12;C14;C16 . . . C18 incl.;C27 = 100n
C25;C26 = 47p polystyrene/styroflex
C28 . . . C31 incl. = 22n

Semiconductors:
B1 = B80C1500 (80 V; 1.5 A bridge rectifier) (Universal Semiconductor Devices; C-I Electronics)
D1 . . . D13 incl. = 1N4148
D14 . . . D23 incl. = 3 mm LED in S1 . . . S10 (ITW switch)
T1;T2 = BC547B
IC1 = 4011
IC2 = 4013
IC3;IC4 = 4028
IC5 = ULN2804A (Sprague)
IC6;IC7 = OP-227GY (PMI) or OP-227GN/GJ (Linear Technology)
IC8 = 7812
IC9 = LM325N

Miscellaneous:
S1 . . . S10 incl. = Momentary action key with hole for LED. Type with broad cap (17.3 mm); ITW Licon series. ITW Switches • Division of ITW Limited • Norway Road • Hilsea Industrial Estate • Portsmouth PO3 5HT. Tel.: (0705) 694971. Telex: 86374. ITT/Schadow Type Digitast switches may also be suitable.
S11 = single-pole mains switch.
F1 = 100 mA delayed action fuse
PCB-mount fuse holder for F1.
K1 = mains entrance socket.
K2 = 3-way PCB terminal block.
K3 = 20-way male PCB header.
One 20-way female flatcable connector (IDC type).
Two 10-way female flatcable connectors (IDC type). Approx. 15 cm of 20-way flat ribbon cable, or two lengths of 10-way cable.

DIL-style heat-sink for IC8.
Tr1 = PCB-mount mains transformer; 2 × 15 V; 8 VA.
PCB Type 880132-

PCB Type 880132-2

References:

(1) Top-of-the-range Preamplifier — *Elektor India*, Dec. 1986, Jan/Feb 1987.

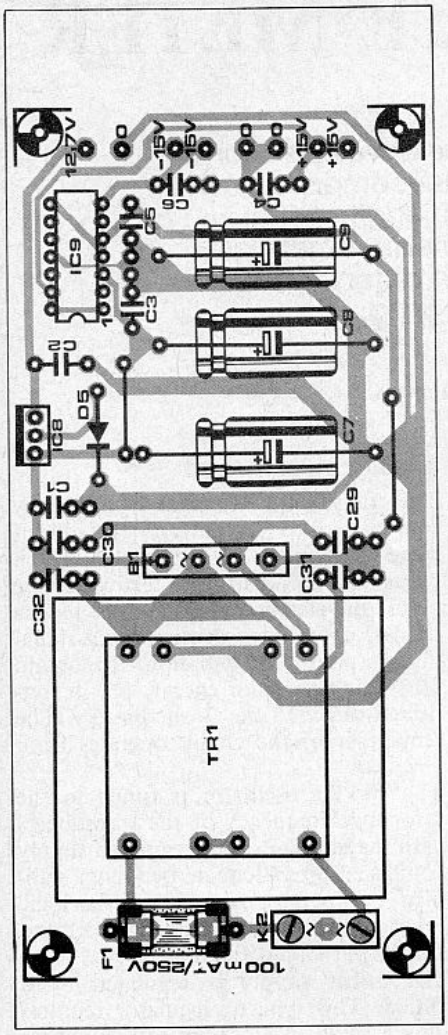


Fig. 10. Component layout of the control board.

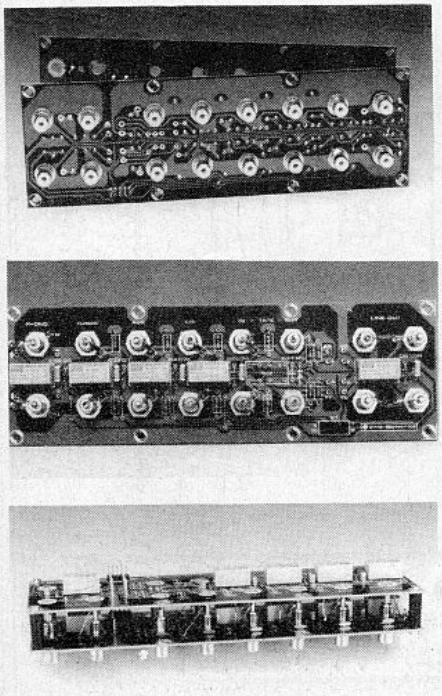


Fig. 11 . This is how the two bus boards are sandwiched.

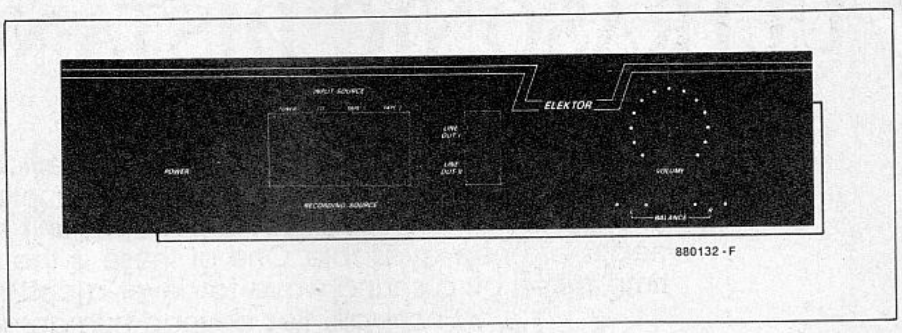


Fig. 12. Foil for the front panel.

When the preamplifier is switched on, the decoders are automatically set to 0, because their inputs are connected to ground (=0) via resistors. In this state the decoder will remain inactive until one of the switches is pressed. If it is desired that one of the inputs is active on switch-on, a 100 n capacitor should be connected across the relevant switch.

Power supply

The circuit of the power supply is shown in Fig. 5. The supply for the control circuits and the relays is stabilized by IC_8, a Type 7812 that has been 'elevated' to a 12.7-V regulator with the aid of D_5. This is done to compensate the voltage drop across the outputs of IC_5, so that the full 12 V remains available for the relays.

The symmetrical supply for the buffer-amplifier is regulated by IC_9.

Any mains noise is filtered by capacitors shunting the diodes of bridge rectifier B_1.

All parts of the power supply, except the mains on-off switch and K_1, are housed on the PCB shown in Fig. 10.

Construction

The two bus boards are mounted one above the other at a distance of about 20 mm. This ensures that terminals A to N incl. are opposite one another, which facilitates inter-wiring them.

The component population plan of the two boards is shown in Fig. 6 and Fig. 8. To facilitate the interconnection of terminals A to N, soldering pins should be used on bus board 1 at the 14 positions indicated. These pins should, of course, be put in place before the resistors of the input potential dividers are mounted. On bus board 2, solder a short length of wire to terminals A to N. These lengths of wire are later soldered to the corresponding soldering pins on board 1.

Before the two boards are finally connected together, solder appropriate lengths of wire to terminals VR and VL on bus board 1: these points are difficult to get at after the sandwich has been formed.

Once the two boards have been made into a sandwich, they may be mounted to the inside rear panel of the preamplifier by eight screws. This number of screws is necessary to spread the mechanical load evenly over the boards.

The component mounting plan for the control and amplifier board is shown in Fig. 9.

Note that switches S_1 to S_{10} must have two terminals for the mother contact, because the connection between these two serves as a wire link in some of the switches.

The board provides three common terminals per channel for the volume and balance controls. The connections between these controls must therefore be hard-wired.

Always begin work on PCBs with placing the required wire links: these are easily forgotten once the board has been populated.

Note that header K_3 and the 1 μF polycarbonate (polyproylene) capacitors should be fitted at the track side of the board. In some cases, it may also be advantageous to locate solder pins at the track side.

Any wiring carrying audio signals is best made in single screened audio cable. The screens may be earthed at both sides, since the boards have been designed to prevent earth loops.

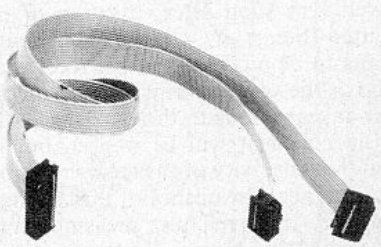


Fig. 13. Flat cable connecting the control board to the two bus boards.

Connections between the control-board and the relays on the bus boards are made by a short length of 20-way flat cable — see Fig. 13. One end of the cable is terminated into a 20-way connector and the other end into two 10-way connectors.

Finally, all identically named terminals on the power supply board and the control board should be interconnected.

ULTRASONIC DISTANCE METER

Until well into the twentieth century, most devices developed for measuring distance worked on the same principle: comparison of the measured distance with a standard unit of length. Other means are now available. One of these is the measurement of time taken by a sound wave to cover a certain distance. This sound normally lies beyond human hearing.

The ultrasonic rangefinder presented here is suitable for measuring distances between 25 cm and about 6 m. The measured distance is shown on a 3-digit liquid crystal display—LCD. The low current drawn by the unit makes battery operation possible: a 'LO BAT' reading on the LCD indicates when the battery needs to be replaced.

The block schematic in Fig. 1 shows the four major parts of the meter: a sender, a receiver, a timing and time reference section, and a counter with display.

The transduction element emits bursts of 12 pulses at a frequency of about 40 kHz. This frequency is roughly identical with the resonance frequency of the two transducers, so that some sort of selectivity is obtained at the sensing element. As soon as the first burst is emitted, a bistable is actuated which enables the counter.

Immediately after the burst has been emitted, the unit is switched to reception. The sensitivity of the receiver is a function of time. During and immediately after emission of the burst, the sensitivity is low. Crosstalk between the transduction and sensing elements has, therefore, no effect on the operation of the unit — see Fig. 5. If an echo is received very soon after cessation of the emitted burst, it will be sufficiently strong to be processed by the receiver in spite of the very low sensitivity. An echo that takes a longer time to reach the sensing element will be weaker, but by then the sensitivity of the reciever has become higher. The upshot of this arrangement is that reliable measurements, unaffected by spurious reflections and crosstalk, may be made with relatively simple means.

At the instant the echo is sensed, the bistable is reset and the counter state transferred to the output latch.

Since the clock frequency is 17.05 kHz and the velocity of sound under normal atmospheric conditions may be taken as 341 m s^{-1}, the period of the clock is equal to the time taken by the burst to travel 2 cm i.e., 1 cm forward and 1 cm back. This means that the number of clock pulses counted between the onset of emission of the burst and the sensing of the echo is equal to the number of centimetres between the transducers and the reflecting surface.

Accuracy

The accuracy of the measurement depends on the precision with which time is measured and on the ambient conditions. The speed of sound depends on the atmospheric pressure, the temperature, and the air density. Readers interested in the details of these dependencies are referred to the inset box.

A source of larger errors than caused by atmospheric conditions is the unit itself, mainly due to the incorrect triggering of the receiver. Partly because of the Q factor of the sensing element, it takes a finite time (up to a few periods of the 40 kHz signal) before the received signal attains maximum amplitude and the receiver is triggered. Each delayed period causes a measuring error of about half a centimetre.

None the less, under normal conditions, measurements made with the prototype at up to 6 m were at all times accurate to within 2%, i.e. 2 cm per metre.

Circuit description

The transduction element is driven by four paired CMOS buffers. The output stage is actually a full bridge which causes a doubling of the effective voltage across the element. Capacitor C_1 blocks the DC component of the output signal during pauses in emission. To obtain bursts at maximum energy, IC_1 is connected direct to the 9-volt battery. The remainder of the circuit operates from 5 V.

The 40 kHz oscillator is tuned to the resonance frequency of the transducers with the aid of P_1. The regulated supply voltage ensures adequate frequency stability. Comparator A_6 matches the logic levels of the oscillator (high = 5 V) and the output circuit (high = 9 V).

The 5-volt supply is regulated by a 78L05. This type of regulator requires only a small bias current at low output currents and thus helps to keep the overall current drawn by the circuit low (typ. 4.5 mA). Unfortunately, the load regulation of this regulator is poor: good decoupling, praticularly of the counter IC (R_{19}–C_{13}), is therefore essential.

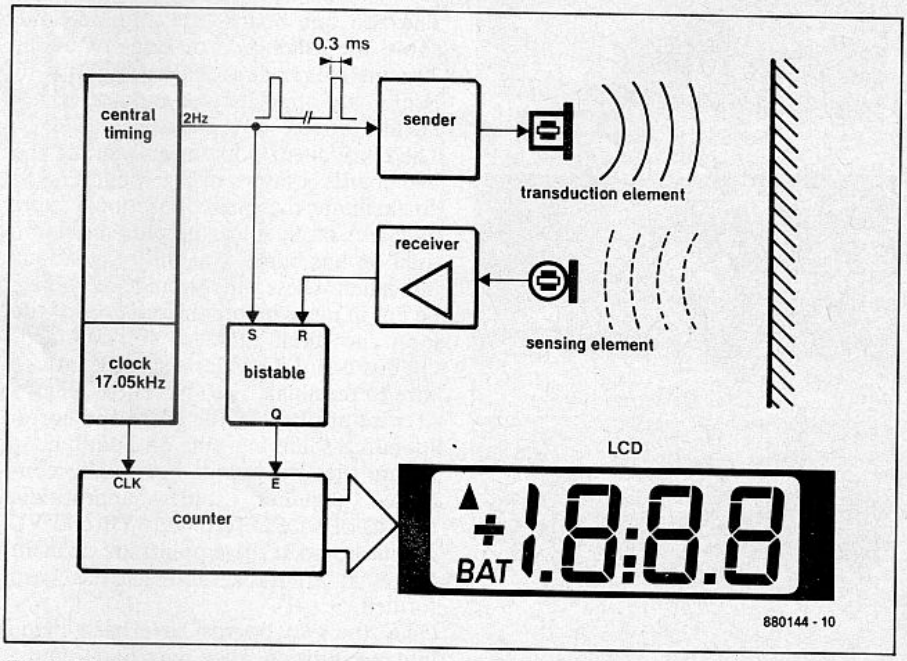


Fig. 1. Block schematic of the distance meter.

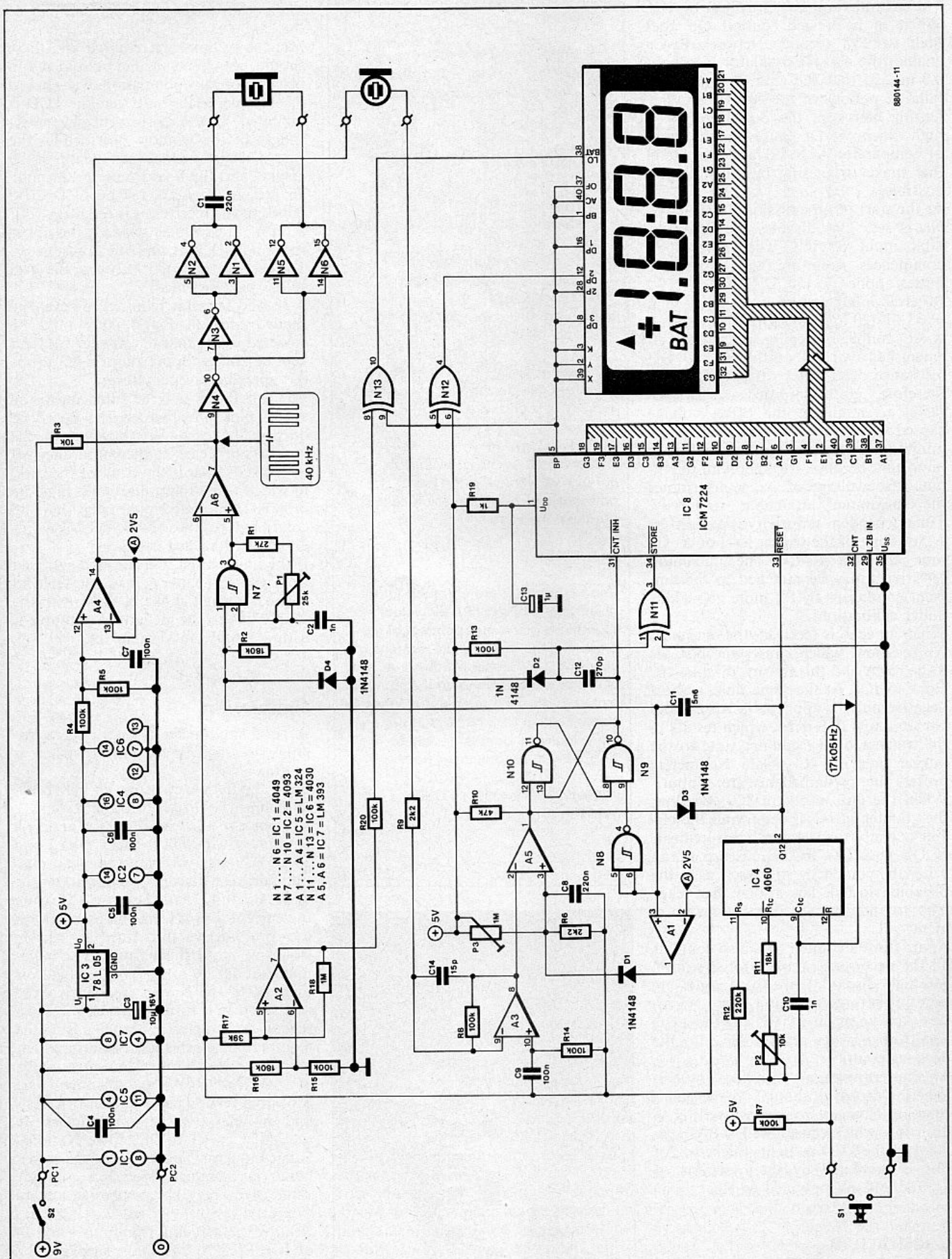


Fig. 2. Circuit diagram of the distance meter.

The central timing is provided by IC_4. When S_1 is pressed, output Q_{12} goes high twice a second. Network R_2-C_{11} enables the 40 kHz oscillator for about 0.3 ms, so that the emitted burst contains 12 periods of the 40 kHz signal.

During emission, the output of A_1 is high which, via D_1, causes the threshold of comparator A_5 to be raised to a level that makes triggering by crosstalk impossible.

At the start of an emission, bistable N_9-N_{10} is set. This disables the count inhibit input of IC_8, which thereupon commences counting the 17.05 kHz pulses applied to pin 32 by IC_4.

Receiver input amplifier A_3 has a gain of 33 dB [20 log(R8/R9)]. The amplifier is AC coupled, because the sensing element has a virtually infinitely high DC resistance. The input offset voltage is, therefore, not amplified. Also, R_{14} serves to minimize the offset voltage caused by the input bias current. A minimum offset voltage at the output is important because, together with the input offset voltage of A_5, it determines the maximum attainable sensitivity. Time-dependent sensitivity is realized by A_1 lowering of the trigger level of A_5 via time constant R_6-C_8. The maximum sensitivity may be matched to the ambient conditions by P_3: more about this under calibration.

When an echo is received, the output of A_5 goes low, which causes the bistable to be reset, and this in turn disables the clock to IC_8. At the same time, a short negative pulse is applied via R_{13}-C_{12} and N_{11} to pin 34 ($\overline{\text{STORE}}$), which results in the transfer of the counter state to the output latch of IC_8. Gate N_{11} merely buffers the low-impedance store input.

When the Q_{12} output of IC_4 goes low, the counter in IC_8 is reset, and the circuit is ready for the next measurement. If Q_{12} goes low in the absence of an echo, the counter is still reset, as is the bistable (via D_3). The display then reads 0.00 to indicate an abortive measurement.

Apart from a counter, IC_8 also contains all the necessary circuitry for driving a 3½-digit display. Only three digits are used in the present circuit. Gate N_{12} inverts the backplane signal of the LCD and thus provides a fixed drive for the decimal point.

The battery voltage is monitored by N_{13}. When it drops to about 7 V, the gate's function changes from non-inverting to inverting, which causes the LO BAT segment of the LCD to light. Flickering of this is prevented by the hysteresis of around 200 mV provided by R_{18}.

Construction

Before anything else, make sure that the printed-circuit board fits snugly in the chosen case. Note that two corners must be removed to allow passage of the screws that fasten the front and rear of the case.

Many wire links are required and these should, as a general rule, be soldered in place before any population of the board takes place. Make sure that the LCD is mounted at the correct height to fit snugly in the window provided in the case. The distance between the top of the display and the board must be 25 mm.

To prevent crosstalk of the LCD drive pulses to the receiver, it is essential to fit a tin or brass screen between the upper row of LCD pins and the transducers. This screen is fitted between the two solder pins provided.

A second screen is required to cover the shaded area in Fig. 4. It should be soldered to the first screen near C_{13}, and kept in place with the aid of a few drops of superglue or epoxy resin.

The tranducers may be fitted on to the solder pins provided on the board or outside the case, for instance, in the bumpers of a car. On the board, they wil be located towards the front of the case, in which two 16 mm dia. holes must be drilled. If mounted externally, they are connected to the board by 2-way individually screened cable.

If the unit is used in a car, and supplied from the car battery, it is advisable to connect a small choke in series with the supply line to the meter and decouple it with a 100 µF, 16 V capacitor.

Velocity of sound in a gas

The velocity of sound, v, in a gas, such as air, for frequencies above 200 Hz, is given by

$$v=\sqrt{(\gamma p/\varrho)}$$

where

γ is the adiabatic bulk modulus of the gas (1.4 for air)
p is the pressure of the gas in Pa (air pressure at sea level is 1.01325×10^5 Pa)
ϱ is the density of the gas in kg m^{-3} (density of air=1.29 kg m^{-3})

If a mole of air has a mass M and a volume V, the density is M/V and the velocity of sound, v, is

$$v=\sqrt{(\gamma p/\varrho)}=\sqrt{(\gamma pV/M)}$$

But $pV=RT$, where R is the molar gas constant and T is the absolute temperature. Therefore,

$$v=\sqrt{(\gamma RT/M)}$$

Since γ, M and R are constants for a given gas, it follows that the velocity of sound in a gas is independent of the pressure if the temperature remains constant. It also follows that the velocity of sound is proportional to the square root of its absolute temperature. Thus, if the velocity in air at 0 °C is 331 m s^{-1}, the velocity at room temperature, 20 °C=293 K, is calculated from

$$v/331=\sqrt{(293/273)}=331\sqrt{1.07326}=342.91 \text{ m s}^{-1}$$

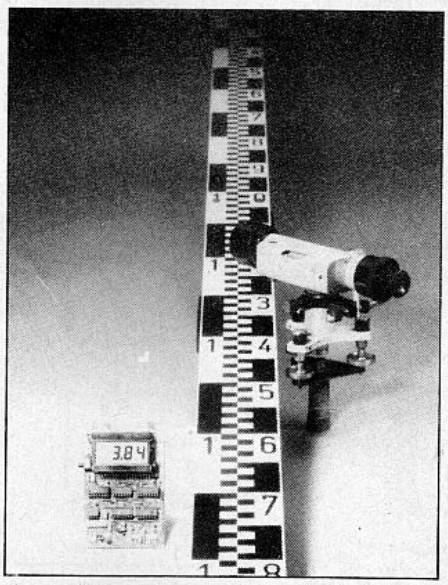


Fig. 3. General view of the distance meter.

Calibration

A good multimeter is essential; an oscilloscope and/or frequency meter is useful.

First, the frequency of the 40 kHz oscillator must be matched to the resonance frequency of the transducers. Connect a temporary wire link between pins 1 and 14 of IC_2: this will cause the transduction element to operate continuously. Turn P_1 fully anticlockwise. Measure the current drawn from the battery with the multimeter and turn P_1 slowly clockwise until the current is a maximum (about 16 mA). The oscillator is then set to the correct frequency. Note that when P_1 is turned further, there is a second current peak, but that is NOT the required point. This is all assuming that the 4093 used in the IC_2 position is of SGS or RCA manufacture. The Motorola version has a smaller hysteresis and this may necessitate an increase in the value of C_2 to 2n2. The National Semiconductor version, on the other hand, has a higher hysteresis, so that the value of C_2 may have to be reduced to 470 p.

Remove the wire link from pins 1 and 14 of IC_2. Press S_1 and make sure that the transduction element produces a short click twice a second.

Next, P_2 must be adjusted until the oscillator in IC_4 operates at 17.05 kHz

Parts list

Resistors (±5%):
R1 = 27K
R2;R16 = 180K
R3 = 10K
R4;R5;R7;R8;R13 . . . R15 incl.;¼R20 = 100K
R6;R9 = 2K2
R10 = 47K
R11 = 18K
R12 = 220K
R17 = 39K
R18 = 1M0
R19 = 1K0
P1 = 25K multiturn preset
P2 = 10K preset V
P3 = 1M0 preset H

Capacitors:
C1;C8 = 220n
C2 = 1n0 (see text)
C3 = 10 µ; 16 V; tantalum
C4 . . . C7 incl.;C9 = 100n
C10 = 1n0
C11 = 5n6
C12 = 270p
C13 = 1µ0; 6.3 V; tantalum
C14 = 15p

Semiconductors:
D1 . . . D4 incl. = 1N4148
IC1 = 4049
IC2 = 4093 (see text)
IC3 = 78L05
IC4 = 4060
IC5 = LM324
IC6 = 4030
IC7 = LM393
IC8 = ICM7224

Miscellaneous:
U1 = MA40A5S ultrasonic transmitter (Murata+)
U2 = MA40A5R ultrasonic receiver (Murata+).
3½-digit LC display with LO-BAT indication.
S1 = push-to-make button.
S2 = miniature SPDT switch.
2 off 20-way contact strips for mounting LC display.
Hand-held ABS enclosure: e.g. BICC-Vero Type 65-2996H (BICC-Vero Electronics Limited • Parr • St. Helens • Merseyside WA9 1PR. Tel.: (0744) 24000). Alternative type: W81*.
Press-on clip for 9 V PP3 battery.
PCB Type 880144

*Listed by ElectroValue Limited • 28 St Judes Road • Englefield Green • Egham • Surrey TW20 0HB. Telephone: (0784) 33603. Telex: 264475. Northern branch: 680 Burnage Lane • Manchester M19 1NA. Telephone: (061 432) 4945.

+ Murata Electronics (UK) Limited • 5 Armstrong Mall • Southwood • FARNBOROUGH GU14 0NR. Tel.: (0252) 523232. Telex: 858971. Fax: (0252) 511528.

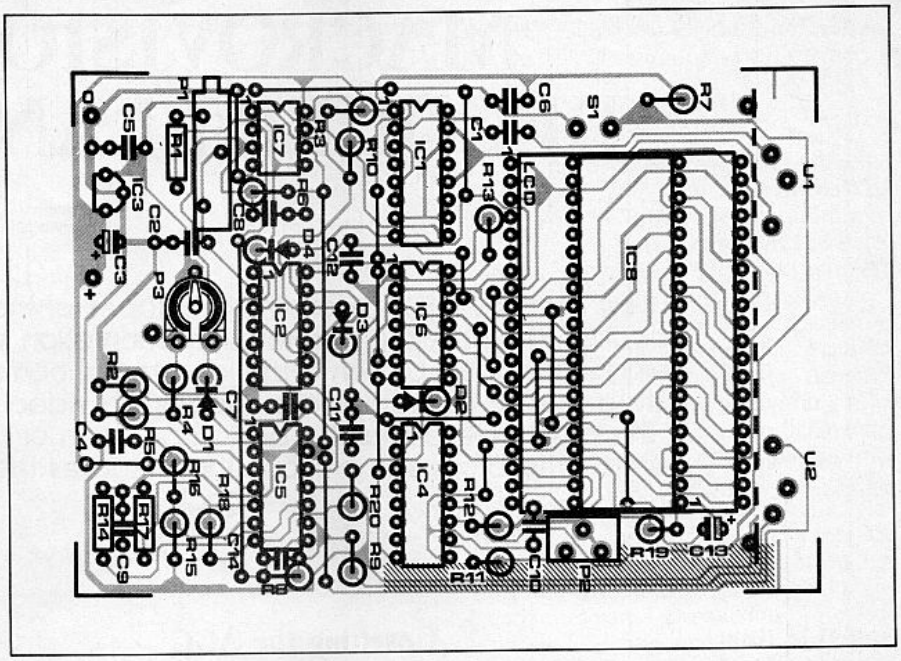


Fig. 4. Component layout of the printed-circuit board.

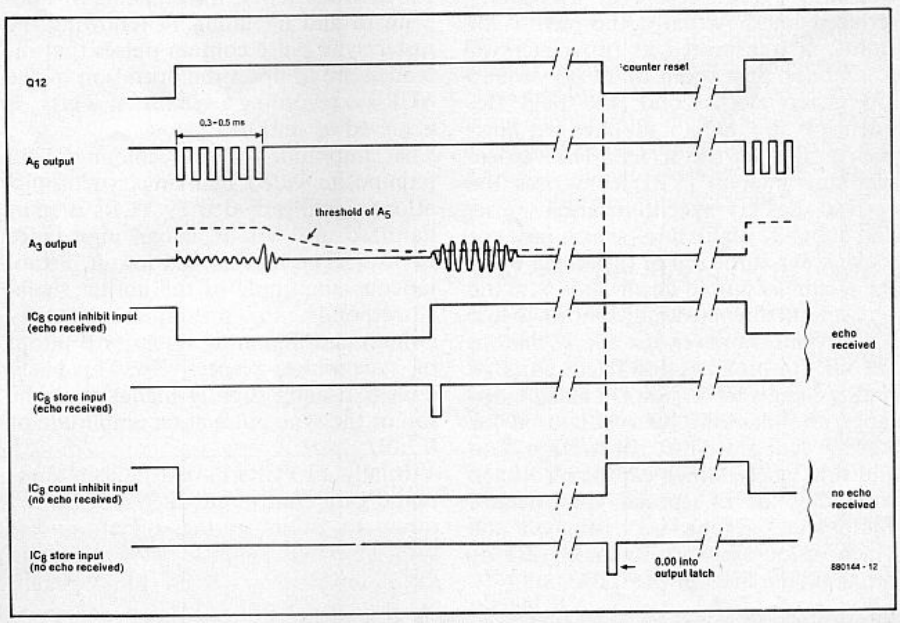


Fig. 5. Timing diagram of the measuring process.

(measured with a frequency meter at pin 9 of the IC). In the absence of a frequency meter, place the unit in a position where the distance between the front of the transducers and a good reflecting surface (a wall or window pane) is exactly one metre (measured with a tape rule or similar). Press S1 and turn P2 until the display reads 1.00. If the reading is not stable or just 0.00, turn P3 slightly until a correct, stable reading is obtained.

Adjustment of P3 (sensitivity) depends largely on the circumstances of use. In quiet surroundings, the control may be set fully anticlockwise (maximum sensitivity). If, however, the display gives spurious readings, like 128, 256, or 512, the sensitivity is too high: the meter then detects its own clock. This is obviated by turning P3 slightly clockwise.

If the unit is used in noisy surroundings, reduce its sensitivity even further, so that it does not respond to spurious sounds. Note, however, that the maximum measureable distance is then reduced.

It should be borne in mind that absorbent surfaces, such as furniture, dressed people, and so on can not, or at least not reliably, be detected. This is because the echo from them is too weak to trigger the receiver. It pays, however, to experiment. For instance, the sensitivity of the receiver may be increased (within reason) by reducing the value of R6. Furthermore, the time dependency of the sensitivity may be altered by changing the value of time constant R6-C8. Reducing that value makes the meter more sensitive over shorter distances.

MACROVISION DECODER/BLANKER

First used by CBS-Fox on PAL VHS tapes of the action movie *Crocodile Dundee*, the MacroVision encryption system is gradually being introduced by film and video rental companies to prevent customers making copies of prerecorded video tapes.
This article describes the basic operation of the MacroVision system, and proposes a circuit that negates the copy protection signal.

Invisible lines

In the PAL system, a television picture is transmitted (and recorded) as 625 interlaced lines. Actually, the picture, or frame, is transmitted as two rasters of 312.5 lines, at a speed of 25 per second (50 rasters per second: the field frequency is 50 Hz). Not all lines are, however, visible on the screen. The vertical blanking interval (VBI) comprises the vertical (raster) synchronization pulse, and about 17 blank lines, which produce a black bar at the top of the screen when the picture is shifted downwards with the vertical picture position control. Most TV stations, however, use the 17 lines in the VBI for broadcasting Teletext and/or timing signals for VCRs. On many video tapes, the blanking interval is used for storing coded product registration data and title labels, which can be read back with the aid of special, proprietary, equipment. Not surprisingly, the MacroVision system also makes use of the available lines in the VBI.

Upsetting the AGC

On the latest releases of MacroVision encoded video tapes, the contents of lines 5 up to and including 14 following the raster sync pulse contain pulses that intended are to upset the operation of the VCR's recording circuits. This is achieved as outlined below.
The amplitude of the colour CVBS (composite video blanking synchronisation) signal provided by VCRs is standardized at 1 V_{pp} at a load impedance of 75 Ω. The highest and lowest instantaneous amplitude of the output signal corresponds to maximum intensity (white) and minimum intensity (bottom of sync pulse) respectively. The black level is usually slightly higher than the top of the sync pulse at an amplitude of 0.3 V.
Virtually all VCRs have a built-in automatic gain control circuit (AGC) at the input to optimize the signal-to-noise ratio by making sure that the recording amplifier is driven with the standard signal amplitude. Most of these AGC circuits are capable of correcting input amplitudes between 0.5 V_{pp} and 2 V_{pp}, and it is precisely this characteristic that is 'exploited' by the MacroVision system. Figures 1a, 1b and 1c show a number of picture lines with different contents. Fig. 1a is the reference, showing the well-known staircase test signal. The line starts with the line synchronisation pulse, followed by the so-called rear porch, which serves as the black reference (in a colour signal, it also carries the colour burst). Then follows the actual picture contents, represented here as the staircase (compare this to Fig. 1b, which shows a blank line). The MacroVision signal is shown in Fig. 1c. It is composed of 5 black-to-white transitions at a frequency of about 48 kHz, with 'black' going lower than the reference level, and reaching down to the bottom of the sync pulse, while 'white' has about two times the amplitude of the standard white level. It will be clear that almost any AGC will fail to correct the amplitude of such a signal, whose interfering effect is further boosted by variation of the maximum white level.

A prototype of the MacroVision decoder/blanker housed in an ABS enclosure.

The AGC circuits in most VCRs use the sync pulse as the reference for setting the amplitude of the video signal. The rear porch level is measured with respect to the bottom of the sync pulse, and set to about 0.3 V. In the lines affected by a MacroVision anti-copy burst, the lowest level of the signal equals that of the sync bottom, causing the recording VCR to mistake these levels for sync pulses. This, in turn, causes the AGC to set the input amplifier gain on the basis of the next black level, which is not a black level at all, but a maximum white level. The AGC can not but reduce the signal amplitude to such an extent that the picture becomes dark, and difficult to synchronise properly. The ultra-white level of the MacroVision may also wreak havoc with

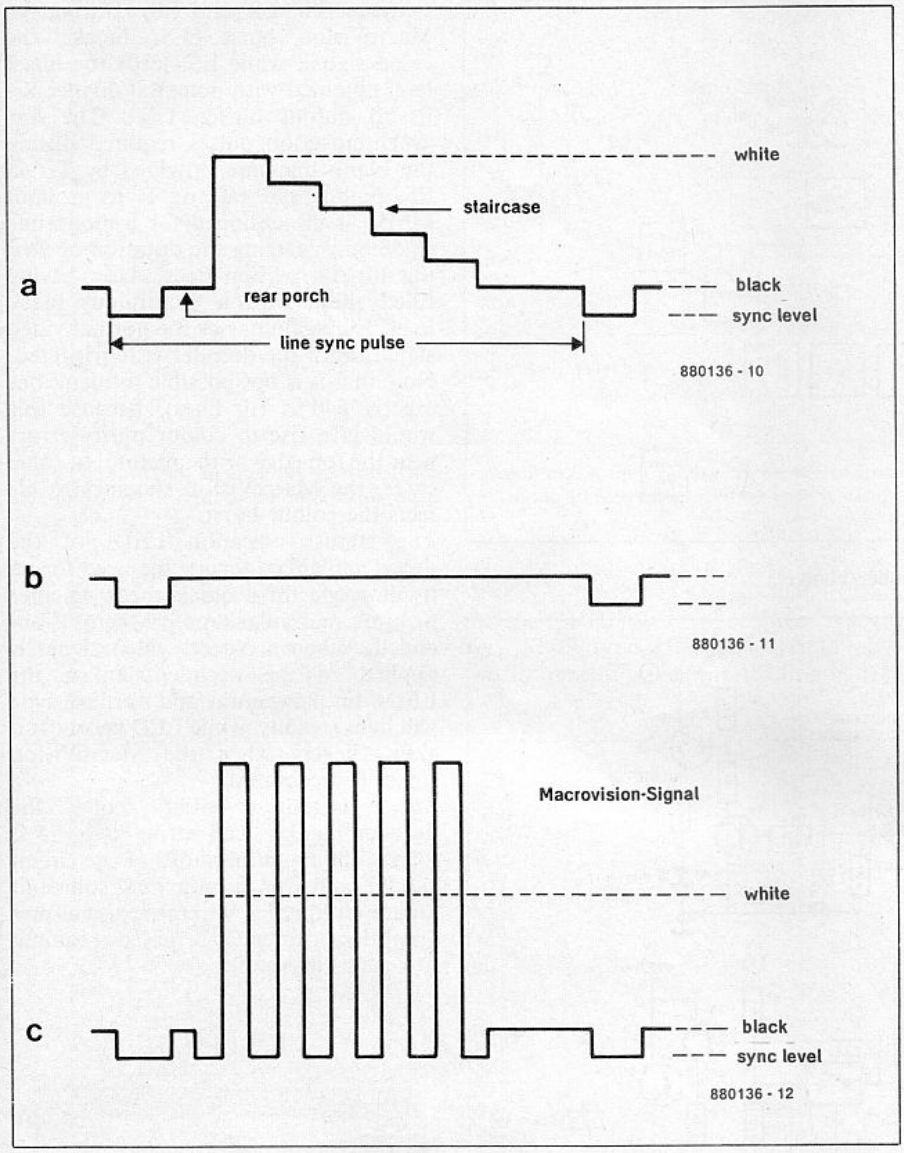


Fig. 1. Staircase test signal (1a), blanked line (1b) and MacroVision interference signal (1c).

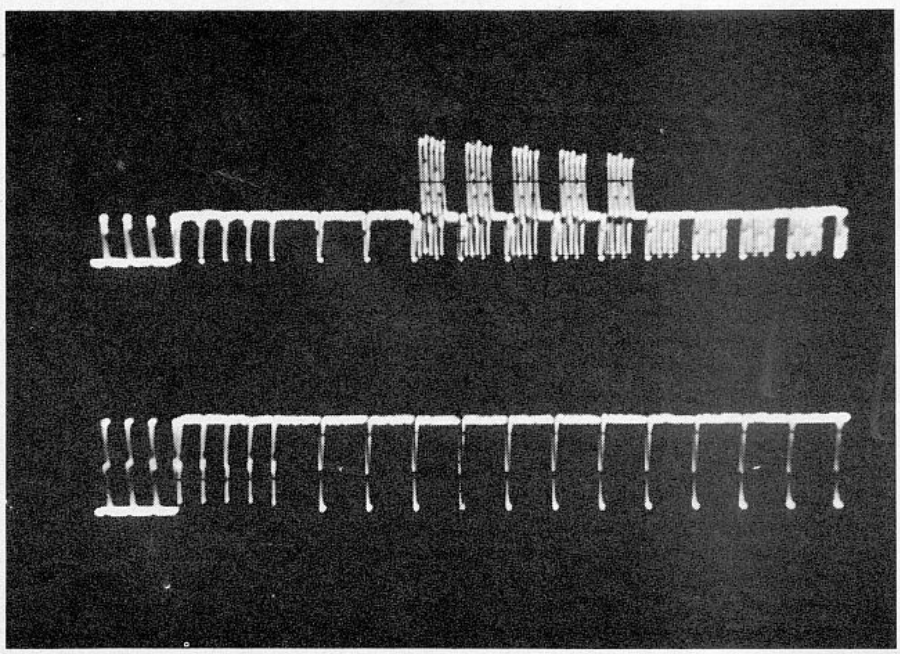


Fig. 2. Double-trace oscillogram showing a line with MacroVision interference (upper trace), and a normal, empty line in the blanking interval (lower trace).

the AGC's overdrive protection, reducing the signal amplitude even further.

Not always effective?

The degree of interference caused by the MacroVision anti-copy burst in the VBI varies from VCR to VCR. In addition to this fact, it is noteworthy that the burst appears to affect VCR input circuits only, not those of most TV sets.

It will be clear from the above discussion that the effect of the interference caused by the MacroVision bursts depends mainly on the dynamic behaviour of the AGC circuit in the VCR. This behaviour, in turn, is defined by the regulation time constants of the circuit. Some VCRs have a 'fast-acting' AGC, others a relatively 'slow' circuit. The latter types are largely insensitive to the pulses in the VBI, and can be used for copying tapes even if these are MacroVision-protected. Modern TV sets generally do not suffer from instability caused by MacroVision-coded signals because the operation of the internal, PLL-controlled, line sync generator is usually not affected by the interfering pulses — hence, the reference black level is correctly deduced from the input signal. Also, there is no input overdrive protection circuit that controls the AGC — signal levels exceeding maximum white are simply clipped.

MacroVision decoder/blanker

The task of the decoder/blanker is to recognize the MacroVision anti-copy burst in 10 successive lines in the VBI, and replace it with a blank (black) level, hence the name *decoder/blanker*. Relatively simple to formulate, this task is not at all simple to carry out in practice. The circuit proposed here is fairly complex because it was purposely designed around discrete, commonly available, components rather than (expensive) special ICs.

The operation of the decoder/blanker is explained with reference to the block diagram of Fig. 3 and the circuit diagram of Fig. 4. At the input of the circuit, T_1 and T_2 form a buffer with an amplification of 2. The signal is then clamped by D_1, so that comparator IC_2 (a BiMos opamp Type CA3130) can filter out the line (H) and raster (V) synchronisation pulses. The line pulses control ES_4 after being filtered in C_5-L_2-T_5. Similarly, the raster pulses reach T_6 after passing through an L-C low-pass filter. The raster pulses at the start of the blanking interval serve to define the time slot available for 'capturing' the MacroVision signal. The positive edge of the raster pulse triggers monostable MMV1, which introduces a delay of 300 μs to time the fourth line, at which the interference starts (see Fig. 5). After the delay has lapsed, MMV_2 is triggered. Its output controls electronic

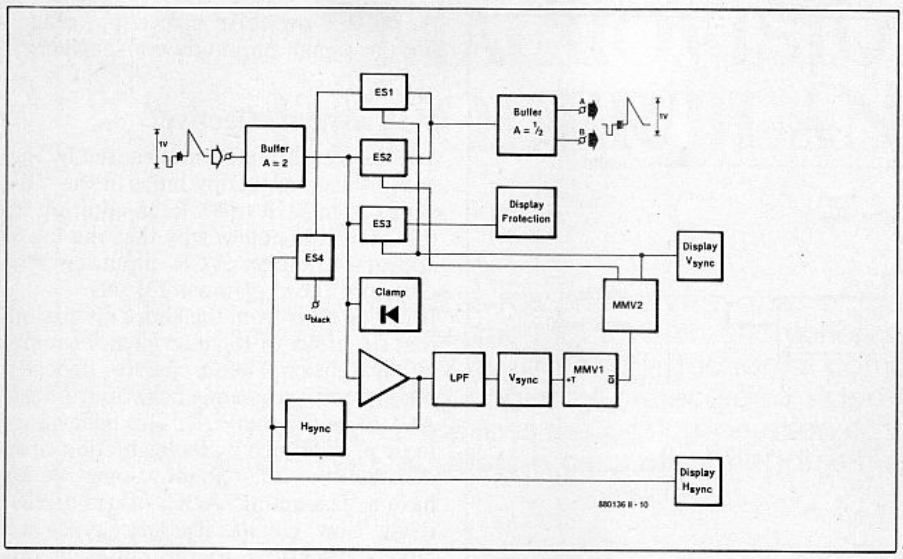


Fig. 3. Block diagram of the MacroVision decoder/blanker.

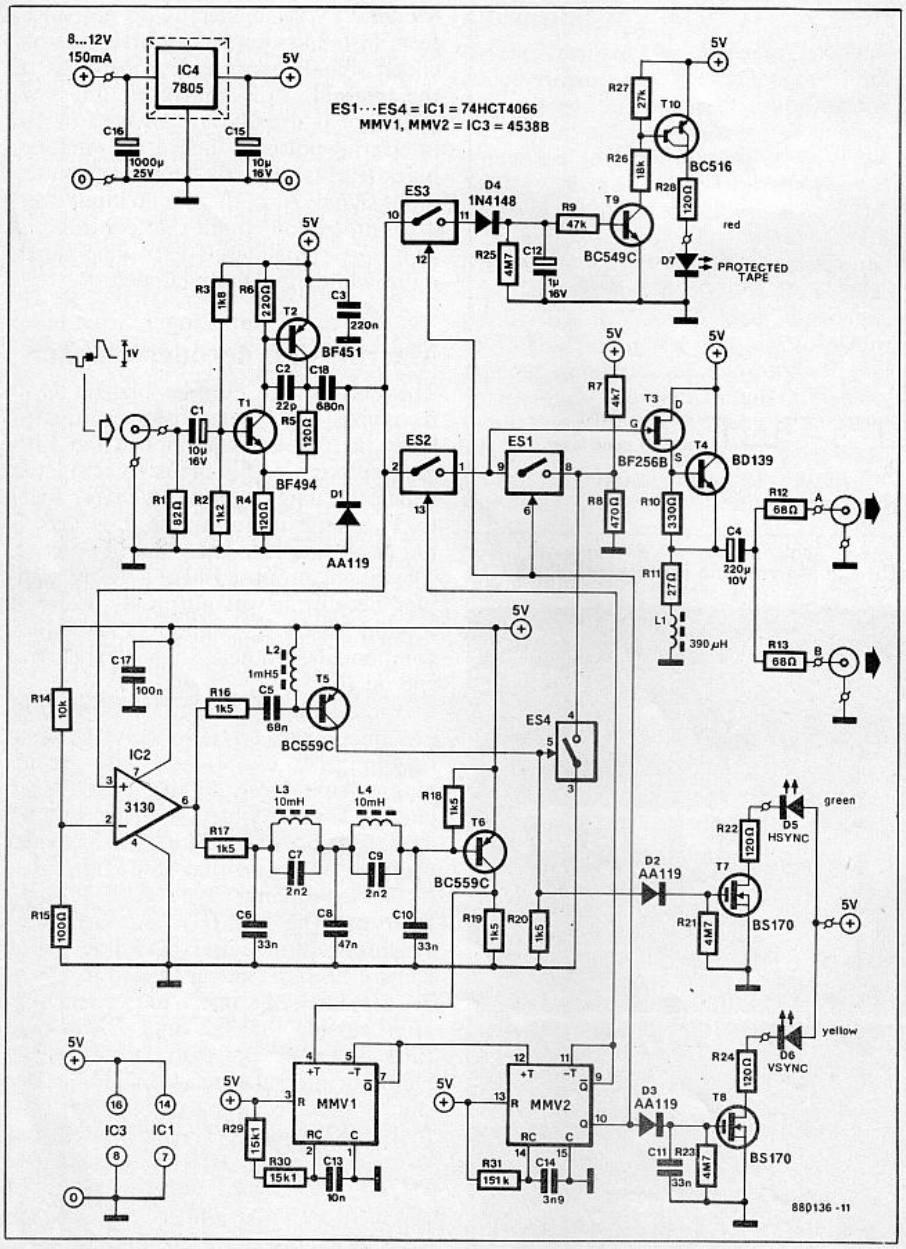


Fig. 4. The low-cost MacroVision decoder/blanker has no adjustment points, and is constructed entirely with discrete components.

switches ES_1, ES_2 and ES_3. During the MacroVision burst, ES_2 breaks the video signal, while ES_1 feeds the black level obtained with potential divider R_7-R_8 to output buffer T_3-T_4. The line synchronisation pulses required during the blank lines are provided by T_5 via ES_4 pulling the gate of T_3 to ground. MMV_2 is dimensioned for a monotime of 589 µs, covering the duration of 9 of the 10 Macrovision lines. After having filled these with a continuous black level, ES_2 again passes the normal video signal, until the decoder is re-triggered. Note that it is not possible to blank out exactly 640 µs (10 lines), because this would give rise to colour purity errors near the top edge of the picture. In some cases, the MacroVision system also affects the colour burst.

The status indication LEDs of the decoder/blanker obviate the need for an oscilloscope for a quick check whether or not a particular tape is MacroVision-coded. When a correct video signal is applied to the decoder/blanker, the LEDs for horizontal and vertical sync will light steadily, while LED PROTECTED TAPE flickers when the MacroVision signal is recognized.

The output buffer of the decoder/blanker can drive two 75 Ω loads. The input amplifier of the circuit should be driven from a 75 Ω source at an amplitude of 1 Vpp (an external preamplifier or attenuator may be required to ensure this level).

No alignment required

The construction of the MacroVision decoder/blanker on the printed circuit board shown in Fig. 6 is straightforward and requires no further discussion other than that it is important not to overlook the six wire links.

No alignment should be required when the relevant 1% resistors and close-tolerance polystyrene capacitors are used as stated in the parts list. The monotime of MMV_1 and that of MMV_2 are purposely made slighty longer and shorter respectively to compensate tolerances. When the capacitors and resistors in the delay circuits have a tolerance greater

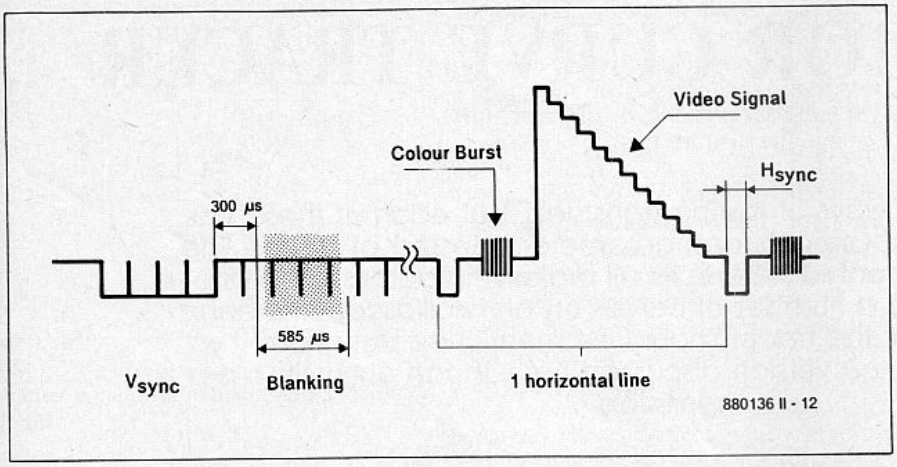


Fig. 5. About 300 µs after the vertical synchronisation pulse, the decoder circuit uses a time slot of 585 µs to replace the interfering pulses in 9 of the 10 MacroVision lines with a steady black level.

than 5%, some MacroVision interference may get through to the recording VCR because ES_2 either shuts down too late, or passes the video signal too early. In this case, R_{30} and R_{31} may be made adjustable (use 10-turn presets) to enable accurate adjustment of the delay times. It is possible to use a 74HC4066 instead of the 74HCT4066 in position IC_1. A LOCMOS type HEF4066 should also work, but this was not tested in practice.

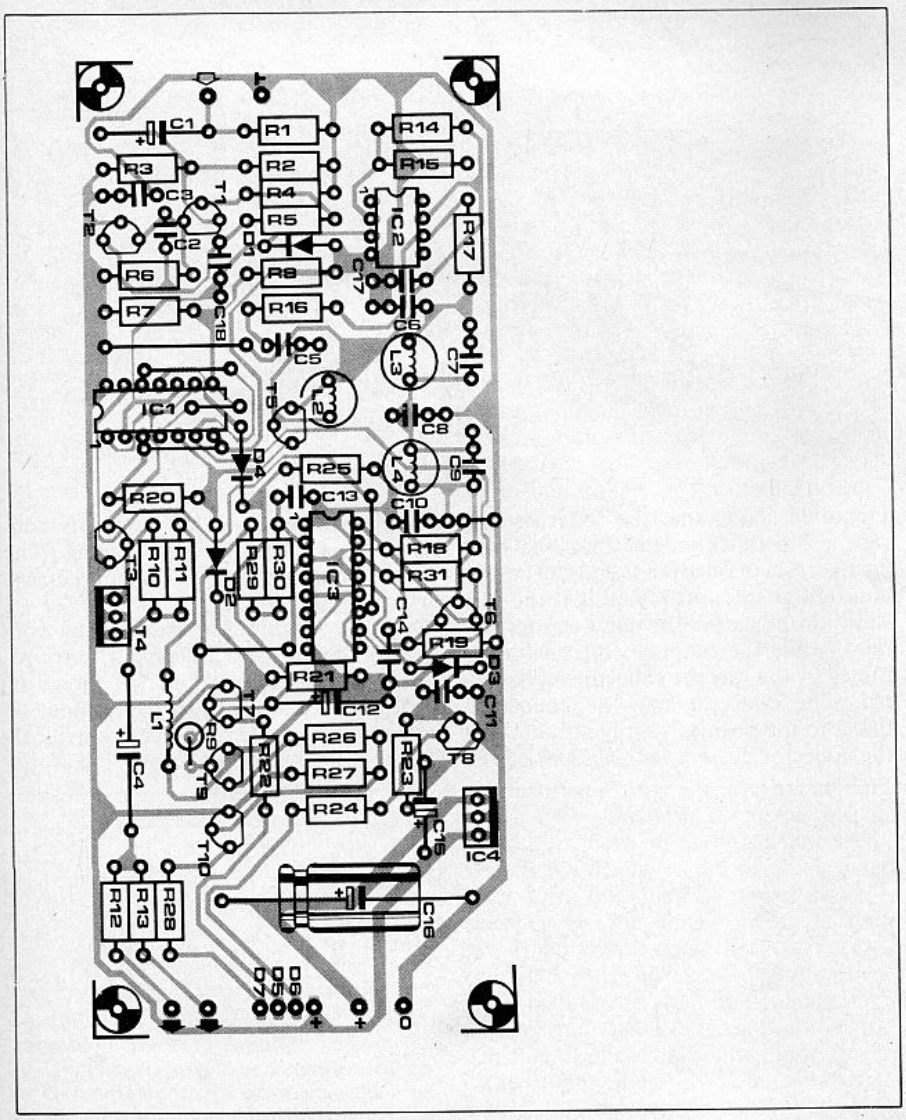


Fig. 6. Track layout and component overlay of the printed circuit board for building the MacroVision decoder/blanker.

Parts list

Resistors (±5% unless otherwise stated):

R_1 = 82R
R_2 = 1K2
R_3 = 1K8
R_4;R_5;R_{22};R_{24};R_{28} = 120R
R_6 = 220R
R_7 = 4K7
R_8 = 470R
R_9 = 47K
R_{10} = 330R
R_{11} = 27R
R_{12};R_{13} = 68R
R_{14} = 10K
R_{15} = 100R
R_{16} . . . R_{20} incl. = 1K5
R_{21};R_{23};R_{25} = 4M7
R_{26} = 18K
R_{27} = 27K
R_{29};R_{30} = 15K1 1%
R_{31} = 151K 1%

Capacitors:
C_1;C_{15} = 10µ; 16 V
C_2 = 22p
C_3 = 220n
C_4 = 220µ; 10 V
C_5 = 68n
C_6;C_{10};C_{11} = 33n
C_7;C_9 = 2n2
C_8 = 47n
C_{12} = 1µ0; 16 V
C_{13} = 10n 5% or better (polystyrene/styroflex)*
C_{14} = 3n9 5% or better (polystyrene/styroflex)*
C_{16} = 1000µ; 25 V
C_{17} = 100n
C_{18} = 680n

* Siemens series B31063 (3n9: ±2.5%; 10n: ±5%). Available from various suppliers, including ElectroValue Limited • 28 St Judes Road • Englefield Green • Egham • Surrey TW20 0HB. Telephone: (0784) 33603. Telex: 264475. Northern branch: 680 Burnage Lane • Manchester M19 1NA. Telephone: (061 432) 4945.

Semiconductors:
D_1;D_2;D_3 = AA119
D_4 = 1N4148
D_5 = green LED
D_6 = yellow or amber LED
D_7 = red LED
T_1 = BF494
T_2 = BF451 (listed by Cricklewood Electronics)
T_3 = BF256B
T_4 = BD139 T_5;T_6 = BC559C
T_7;T_8 = BS170 (listed by Cricklewood Electronics)
T_9 = BC549C
T_{10} = BC516
IC_1 = 74HCT4066 or 74HC4066
IC_2 = CA3130
IC_3 = 4538B
IC_4 = 7805

Inductors:
L_1 = 390µH axial choke
L_2 = 1mH5 radial inductor, e.g. Toko Type 181LY-152 (Cirkit stock no. 34-15202).
L_3;L_4 = 10mH radial inductor, e.g. Toko Type 181LY-103 (Cirkit stock no. 34-10302).

Miscellaneous:
PCB Type 880136

TRANSISTOR CURVE TRACER

There exist many ways of testing transistors, but each of these has its limitations because only one parameter is tested at a time. The curve tracer presented here tests all major characteristics in one go by displaying a number of curves on an oscilloscope screen. One limitation of the tracer should be mentioned right from the start, however: in the version discussed here, it can only test n-p-n transistors.

Background to transistor testing

A simple o.k./faulty test of a transistor can be carried out by considering the device as consisting of two anti-series connected diodes (Fig. 1). This test, which can be carried out with the aid of an ohmmeter, is fine for an initial check, but fails to provide information on one of the most important transistor characteristics: the static forward current transfer ratio, h_{FE}, also referred to as the current amplification.

Most bipolar transistors have 3 terminals: base (B), emitter (E) and collector (C). For the description of their electrical characteristics, however, transistors are often treated as four-pole circuits. This is so because one terminal, usually the emitter, is common to the input and the output (Fig. 2; common emitter circuit). The four-pole circuit of Fig. 2 thus has 2 inputs, base and emitter, and two outputs, collector and emitter. Electrically, there are four important parameters to consider: base input current (I_B), input voltage (U_{BE}), output collector current (I_C), and output voltage (U_{CE}).

Without going into the actual, quite complex, operation of the transistor, it is safe to say that this should convert a base current into a more or less proportionally larger collector current. The conversion ratio is the previously mentioned static characteristic h_{FE}, sometimes also written as a'.

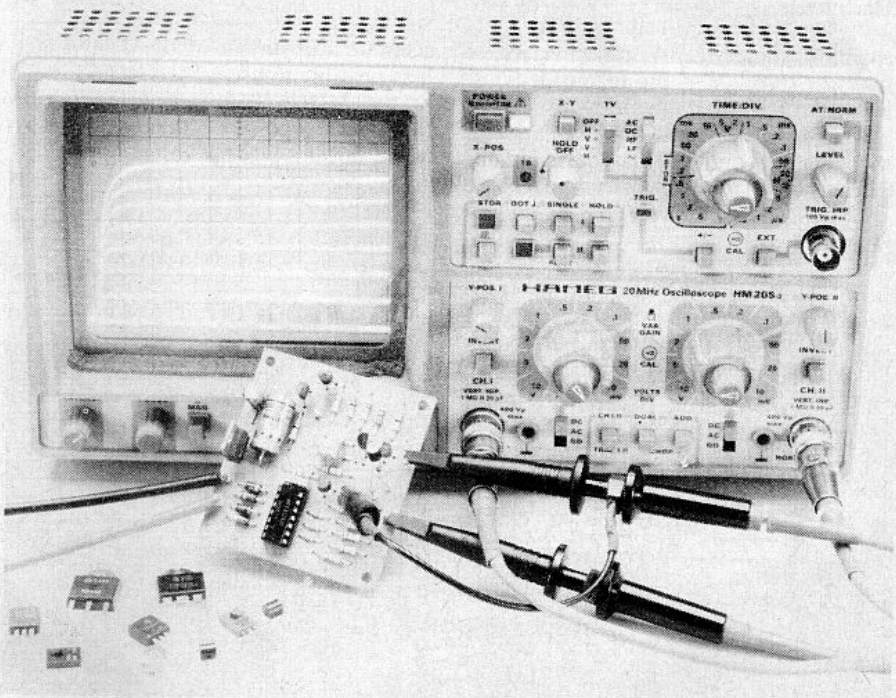


Figure 3a shows that the collector current is h_{FE} times greater than the base current. The base input voltage is largely constant at 0.6 to 0.7 V (this is the forward drop across the base-emitter diode), while the output voltage is determined by the way the collector is connected. The collector may be connected direct to the positive supply rail, making the collector current independent of the supply voltage level, because it is controlled solely by the base current. The circuit thus obtained is called a *current source*.

Output voltage rather than output current is obtained by inserting a series resistor in the collector line as shown in Fig. 3b. This resistor of value R translates the collector current into a collector voltage, and the circuit thus forms

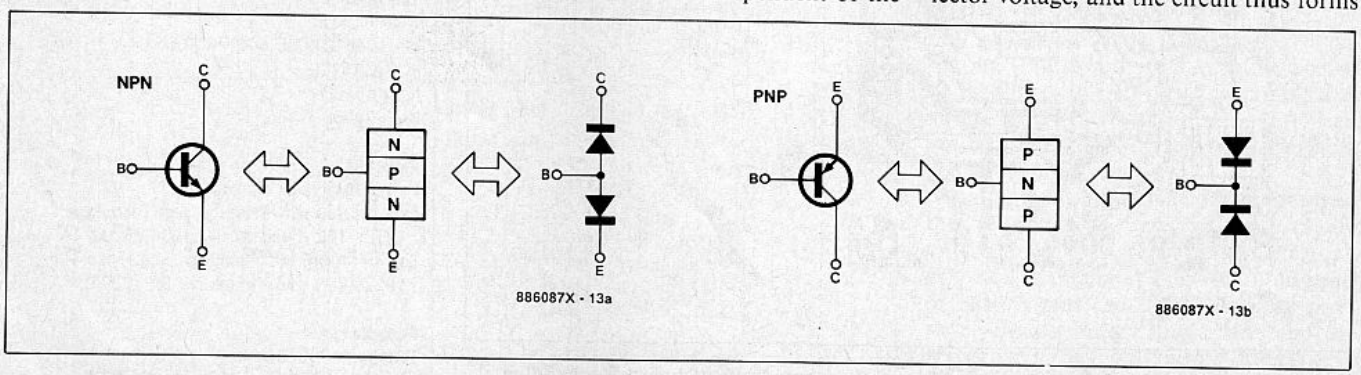


Fig. 1. The simplest way of testing transistors is the ohm-meter check, which is based on the fact that a transistor is essentially formed by two anti-series connected diodes.

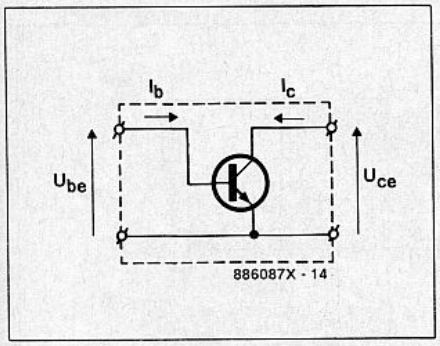


Fig. 2. Transistor as a four-pole circuit. The emitter is common to input (left) and output (right).

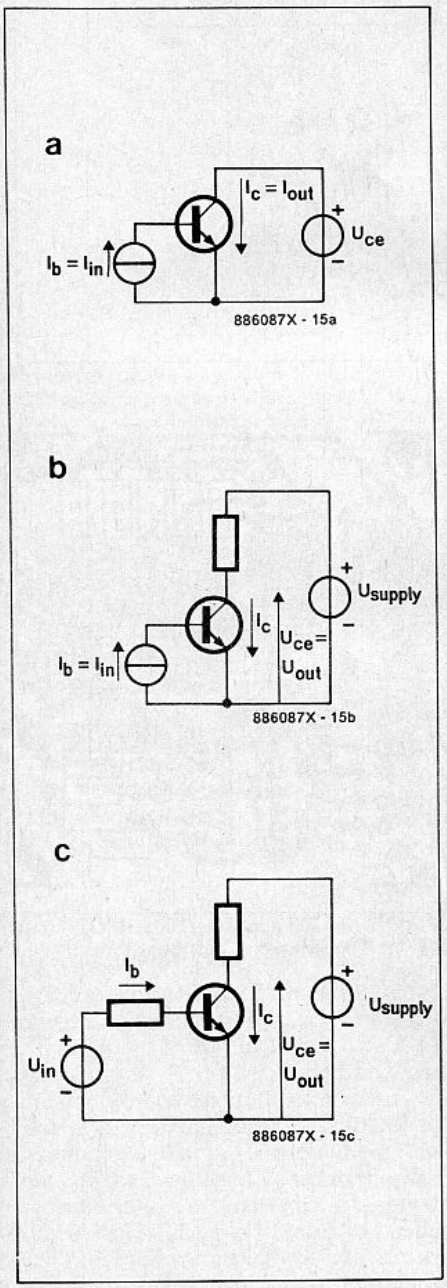


Fig. 3. Basic transistor circuits. Fig. 3a: current-to-current amplifier (I_B-to-I_C). Fig. 3b: current-to-voltage amplifier (collector current is translated in a voltage by a resistor). Fig. 3c: voltage-to-voltage amplifier (input voltage is first converted into a base current by a resistor).

an amplifier which converts input current I_B into output voltage I_CR. Since the voltage on the collector is measured with respect to the emitter, it decreases with increasing base current, so that the transistor works as an *inverting amplifier*.

It is also possible to configure the transistor as a voltage-to-voltage amplifier (Fig.3 c). It is not possible to apply any voltage higher than about 0.7 V direct to the base, because this would cause excessive base-emitter current which is likely to cause destruction of the transistor. To prevent this, a resistor is fitted in series with the base, to convert the input voltage into base current, which, in turn, results in collector current or voltage as discussed above. The input voltage is actually lowered by the fixed base-emitter drop of about 0.6 V. This drop is usually compensated by biasing techniques, which will not be discussed here.

Transistor characteristics

Although many manufacturers provide transistor characteristics in the form of reference tables, it may be more convenient to deduce the exact behaviour of a particular type from plotted curves. Of these, the so-called *output characteristic* is by far the most important. As an example, Fig. 4 shows the output characteristic of the well-known BC107. The curves show the collector current as a function of the collector-emitter voltage, with base current as a parameter. An ideal transistor would produce straight lines — collector current is constant, since its magnitude is governed by the base current only, not by the collector-emitter voltage. The curves show that this is not so in practice. The so-called *early effect* becomes manifest at relatively high values of the collector current, causing the transistor to behave unlike an ideal current source.

Figure 4 can also be used to deduce the current amplification factor. The 50 μA curve gives an average collector current of 12.5 mA, so that $h_{FE} = I_C/I_B = 12.5/0.05 = 250$.

Block diagram

The transistor curve tracer is capable of showing the previously discussed output characteristic on an oscilloscope screen. The curves displayed are of great value for a quick o.k./faulty test, but also for determining the approximate current amplification of unmarked transistors, which are often offered in surplus stores and at rallies at a fraction of the cost of marked and tested devices. Another interesting application of the curve tracer is the finding of closely matched types in a batch of transistors.

With reference to the block diagram of Fig. 5, a sawtooth generator drives an

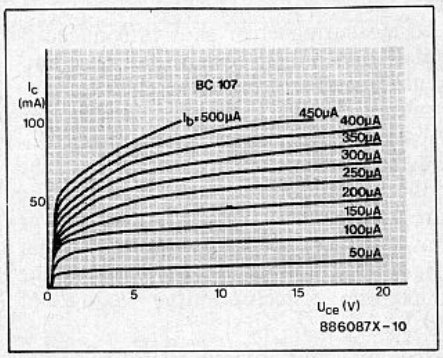


Fig. 4. Output characteristic of the Type BC107 transistor.

amplifier that provides the collector-emitter voltage, which swings between 0 and 10 V. The I_B control block ensures that the base current for the transistor under test is increased in steps of 25 μA. The completely automatic test procedure is cyclic and comprises the following operations:

1. the base current is set, starting at 0 μA;
2. the sawtooth generator gradually raises the collector voltage;
3. when the maximum value of U_{CE} is reached, the sawtooth generator is reset, and the base current is increased by 25 μA;
4. steps 2 and 3 are repeated.

After 8 test cycles, the base current is set to nought again, and the procedure is restarted.

The oscilloscope should really measure both the collector-emitter voltage and the collector current. A different appraoch is required, however, for both measurements. The deviations caused by the approach adopted are acceptable, as will be shown below.

In practice, the emitter current is measured instead of the collector current, as the drop across current sensing resistor R_1. The emitter current is slightly higher than the collector current because it is the sum of the collector current and the base current. Fortunately,

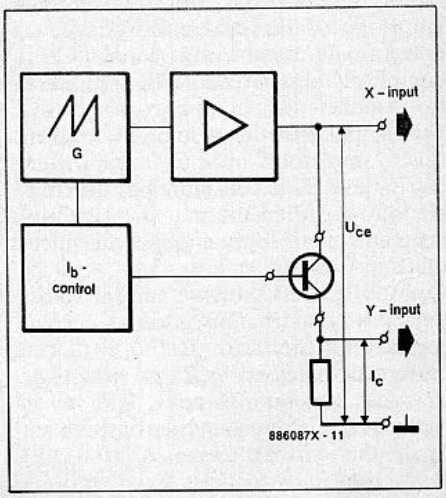


Fig. 5. Block diagram

the measuring error thus introduced is smaller than 1%, because the base current is small relative to the collector current.

A small measurement error is also introduced in the recording of the collector-emitter voltage because the drop across R_1 is included. This resistor has a value of only 1 Ω, however, so that the error amounts to only 0.1 V at the maximum collector-emitter voltage of 10 V.

There are two reasons for not measuring the 'real' collector current and collector-emitter voltage. Firstly, the non-standard arrangement allows the ground reference for the recording instrument (i.e., the scope) to be the same as that for the circuit. Secondly, inversion of the curves on the display is avoided (there are still many oscilloscopes around that lack an invert function on each input).

The sawtooth generator operates at such a speed as to produce apparently non-moving curves on the scope screen (see Fig. 9).

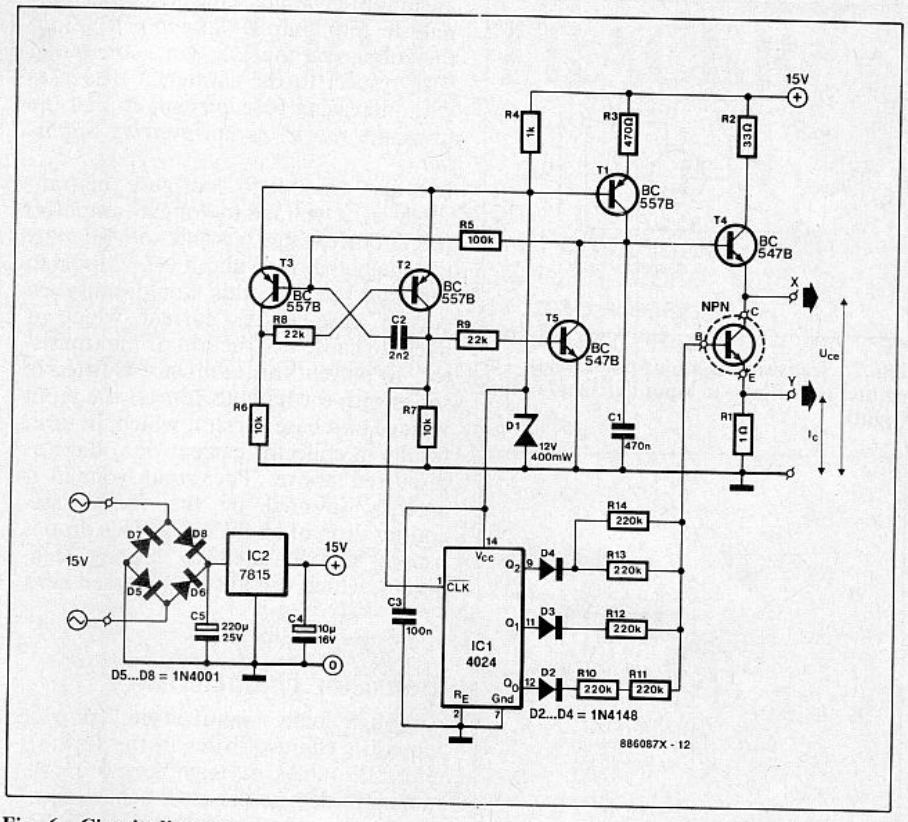


Fig. 6. Circuit diagram

Practical circuit

The circuit diagram of the transistor curve tracer is given in Fig. 6. The rising slope of the sawtooth voltage is provided by current source T_1-R_3-R_4-D_1 and a capacitor. D_1 keeps the base voltage of T_1 fixed at 12 V. The emitter is, therefore at 12.7 V, resulting in a collector current of about 5 mA at the given value of R_3. This current charges C_1 and results on a linearly increasing voltage on the capacitor. T_2 and T_3 monitor the instantaneous output voltage of the sawtooth generator. T_3 conducts via R_5, and T_2 is kept off, until the maximum value is reached. When this happens at $12 - U_{BE(T3)} = 11.3$ V, T_3 is turned off. T_2 can then conduct via R_8 because the collector of T_3 is pulled to the ground potential by R_6. The collector voltage of T_2 rises rapidly to practically 12 V, and causes T_5 to conduct via R_9. T_5 in turn rapidly discharges C_1, forming the falling slope of the sawtooth voltage. C_2 prevents T_3 conducting before C_1 is completely discharged. When T_2 starts to conduct, C_2 supplies a positive voltage pulse to the base of T_3, causing this to remain off until C_1 is completely discharged. T_4 is configured as an emitter follower to ensure that the sawtooth generator can supply enough current to the transistor under test.

Counter IC_1 sets the base current via its binary outputs that function as current sources together with R_{10} to R_{14}. The current is increased by 25 µA when the sawtooth generator is reset, and IC_1 is clocked. Since three counter outputs are used, the current increases in 8 (2^3) steps from 0 µA to 175 µA.

The circuit is fed from a regulated 15 V supply to ensure a stable display.

Parts list

Resistors (±5%):
R1 = 1R0
R2 = 33R
R3 = 470R
R4 = 1K0
R5 = 100K
R6;R7 = 10K
R8;R9 = 22K
R10 . . . R14 incl. = 220K

Capacitors:
C1 = 470n
C2 = 2n2
C3 = 100n
C4 = 10µ; 16 V
C5 = 220µ; 25 V

Semiconductors:
D1 = zener diode 12 V; 400 mW
D2;D3;D4 = 1N4148
D5 . . . D8 incl. = 1N4001
IC1 = 4024
IC2 = 7815
T1;T2;T3 = BC557B
T4;T5 = BC547B

Miscellaneous:
PCB Type 886087

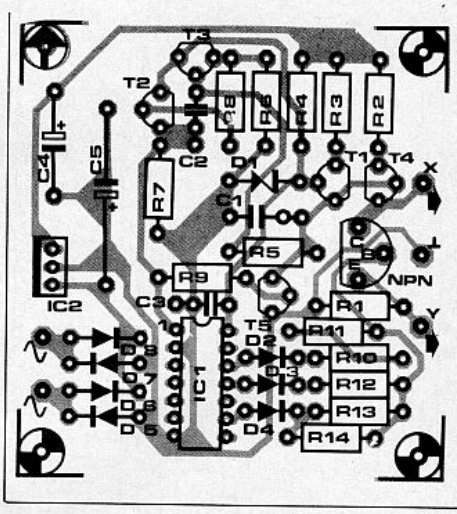
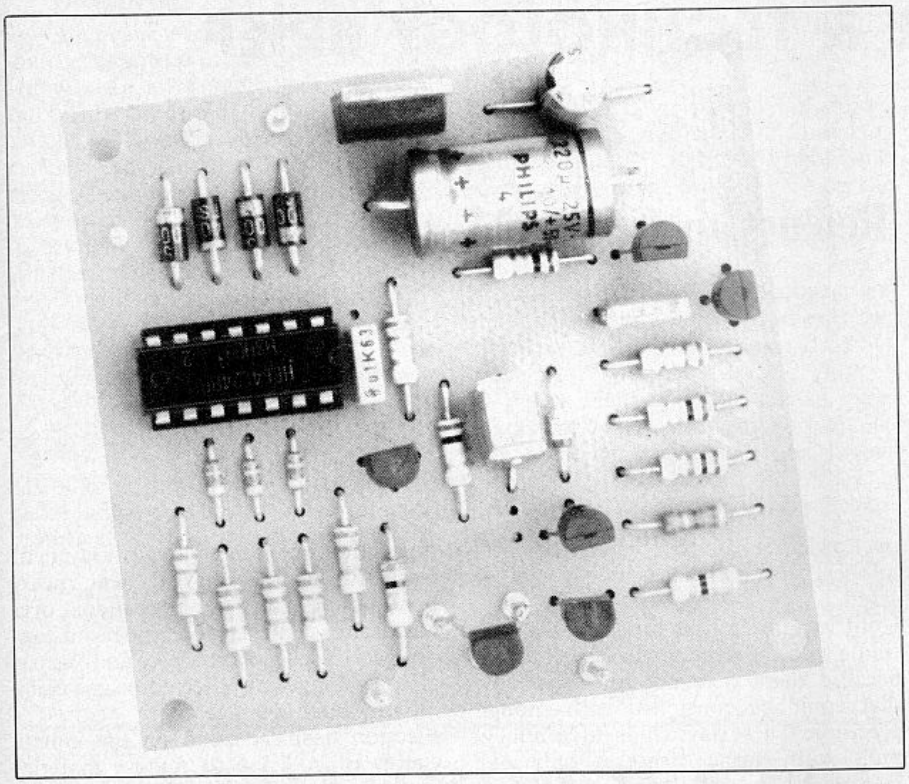


Fig. 7. The printed circuit board



Prototype of the populated board. Note that the ready-made board supplied through the Readers Services has a solder mask at the track side, and a printed, silk-screen, component overlay at the component side.

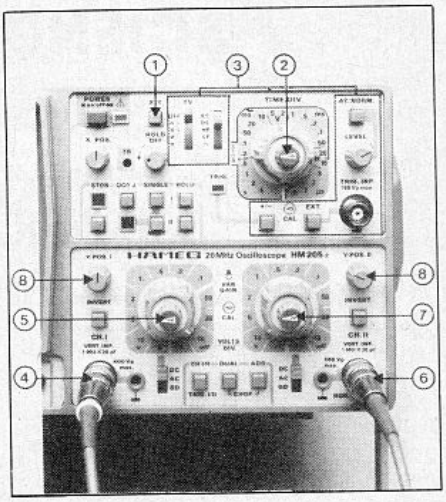


Fig. 8. Typical oscilloscope setting for operation with the curve tracer. 1) X-Y button pressed. 2) Internal timebase off. 3) Trigger circuits disabled. 4) Y input that receives the converted collector current via a 1:1 probe. 5) Input attenuator set to 10 mV/div. 6) Second Y input of the scope used as X input here. 7) X sensitivity set to 1 V/div. 8) Zero reference point of the graph is shifted to left-hand bottom corner of display.

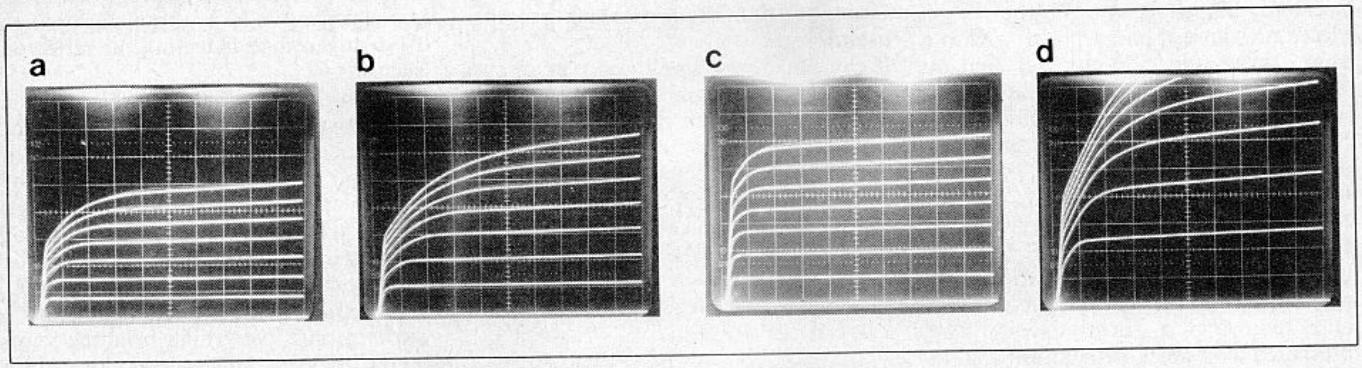


Fig. 9. Some curves obtained with frequently used transistors. From the left to the right: BC547A, BC547B, BC550, BC550C.

Construction and connection to the oscilloscope

Construction of the transistor curve tracer is downright simple on the printed circuit board shown in Fig. 7. Use a 14-way socket for IC_1, and mind the polarization of electrolytic capacitor C_5. The voltage regulator, IC_2, should not require a heat-sink. Connect the AC inputs of the completed board to the 15 V secondary of a small (4.5 VA) mains transformer. The n-p-n transistor under test (TUT) is connected to the tester by means of short, insulated and coloured test wires terminated in small crocodile clips.

The oscilloscope should be set to operate in X-Y mode, in which the built-in timebase is disabled. Connect output X of the tester to the terminal labelled X-EXT or HOR. on the oscilloscope (on some double-trace oscilloscopes, one of the Y inputs can be set to function as X input). Use a 1:1 probe to connect ground and output Y of the tester to the corresponding input(s) of the scope. Since the current sensing resistor has a value of 1 Ω, 1 mA of collector current corresponds to 1 mV. In most cases, the results obtained with the curve tracer are optimum when the scope sensitivity is set to 10 mV per division. Figure 8 shows a typical oscilloscope setting.

Results

Figure 9 shows 4 oscilloscope photographs taken with commonly used transistor types connected to the curve tracer. The rate of rise of the left part of the curves shows the different static characteristics of the transistors. Figure 9a applies to a Type BC547A, Fig. 9b to a Type BC547B. The latter type clearly has a higher current amplification (as indicated by the suffix in the type number). The curves in Fig. 9c belong to a BC550B. The current amplification of this transistor is about equal to that of the BC547B, but the larger part of each curve runs almost horizontal. The BC550B, therefore, comes closer to the ideal transistor than the BC547A or B, and will cause less distortion in an amplifier circuit. The last photograph, Fig. 9d, shows the behaviour of the Type BC550C, which has such high current amplification that some of the curves run off the screen. When transistors with a very high value of h_{FE} are tested, it may be necessary to fit a small switch in series with D_4. When the switch is opened, the maximum base current is 75 rather than 175 μA, and the scope displays only four curves.

Delicate Repairs to Costly Microchips

by Leon Clifford

Delicate microsurgery to repair faulty silicon chips was performed for the first time in Britain in early 1987 by a small high technology company which plans to turn its expertise into a money-spinning business. The company, Oxford Applied Research (OAR) of Witney, is a spin-off from Oxford University with which it still works closely.

The company makes complicated scientific instruments, known as ion beam machines, and its foray into the microchip business happened almost by accident. Engineers at STC, the British electronics group, had a problem with a chip they were developing and it transpired that OAR's ion beam machine could provide the solution.

"It really was a tool looking for a role and then along came STC with this problem and we were able to solve it," said Dr Roy Clampitt, the managing director of OAR. The operation for STC involved using an ion beam machine to make a precise incision on eight prototype chips and removing a short circuit. This prevented a six-week delay in getting the chip into full production.

Dr Clampitt thinks that chip repair is likely to be a growth business. "My challenge now is to break into that market. There is a huge potential," he said.

Surgical precision

There is an explosion in customized or application-specific integrated circuits as more companies are demanding specially tailored chips to fit the electronic systems they are making. An increasing number of different chip designs is being created and they have to be tested as prototypes before volume production commences.

It can take up to two months to turn a design into a prototype and a minor fault that delays prototype testing can result in a costly two-months slip in the manufacture of a new product. However, if it is possible to repair a prototype chip to enable testing to be completed without ordering another batch of prototypes, then time and money will be saved.

Until very recently it was impossible to fiddle with the structure of a silicon chip because there were not tools available that could be controlled with enough precision. These days chips are routinely built with surface features only one micrometer or even less across. So the electronic 'scalpels' that the chip doctors need must be able to make incisions that are on the same scale. That is where Dr Clampitt's ion beam machine becomes useful.

It can make very small and precise cuts by directing a beam of charged atomic particles called ions, on to the surface of a material. Electric fields steer and focus the beam to accuracies of less than a 1 μm. Ion beams have distinct advantages over other cutting beam technologies such as laser and electron.

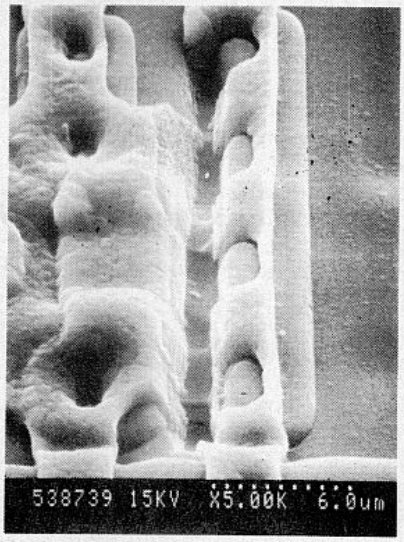
Potential market

Cutting lasers produce a powerful and intense beam of energy which pumps a lot of heat into a small space. The cutting action works by boiling off layers of material but this makes them messy because hot debris can be scattered over a wide area. Furthermore, the beam cannot be focused very precisely and there is also the danger of reflected beams causing unwanted damage.

Electron beams depend on the kinetic energy of collision to remove material but since atoms are much more massive than electrons, electron beams are not very effective. They are more useful as microscopes, and scanning electron microscopes work by bouncing beams off a surface and detecting the reflected electrons.

Ions, on the other hand, have about the same mass as atoms and can deliver a lot more kinetic energy on to a surface. An ion beam depends on the brute force of collision to dig into a material. A high speed ion literally knocks an atom out of the material and a powerful beam of ions van remove material quite rapidly.

Dr Clampitt and his OAR team started working on a 'very high brightness ion source' in 1980. This was developed in a collaborative research programme with Britain's Science and Engineering Research Council. They shared the costs equally. "I directed the project specifically towards milling and etching since from the company's point of view I could see a potential market," said Dr Clampitt.



A cut in the surface of a microchip

Eliminating short-circuits

"What we have here is essentially a scanning ion microscope," he said, "A focused ion beam machine can do everything that a scanning electron microscope can do. It can see things such as a fault on a chip, and we can also use it actually to remove the fault."

The machine can be switched from being a microscope to a cutter simply by making the ions move faster. This is achieved by cranking up the electric fields that accelerate the ions. This ability to use one machine for both looking and cutting is ideal for repairing chips.

The ion beam machine can repair faults that occur in the production of a chip. For example, an unwanted piece of metal can form a conducting bridge — a short-circuit — between two parts of the chip, which makes it useless. However, if this bridge is removed and the short-circuit is broken, then the chips's electrical integrity is restored.

"If it is a metal bridge and if it is accessible, then it can be cut," said Dr Clampitt, "and yet most of the companies that do full custom chip design have never heard of this technique."

Saving the prototypes

STC's problem involved an unwanted metal bridge that had occurred on eight prototypes of a new telecom chip designed by STL, the company's research arm, using 2 μm double-level complementary metal oxide semiconductor (CMOS) very large scale integration (VLSI) technology. "The mighty STC with all its microscopes could see the fault but could do nothing," said Dr Clampitt.

The prototype chips were manufactured in the United States by a semiconductor company, said STL's David Wright, who was in charge of the project. "We got the design right but one mistake was made in the final stages of physical layout in the United States. The chip contains 70,000 devices and 100,000 connections and one of those connections was put down on top of another instead of by-passing it," he explained.

"We had eight chips which we knew would work except for this short circuit. The obvious thing to do was to cut through it," said Mr Wright. The cut needed to be 20 μm long, 2 μm wide and less than 1 μm deep.

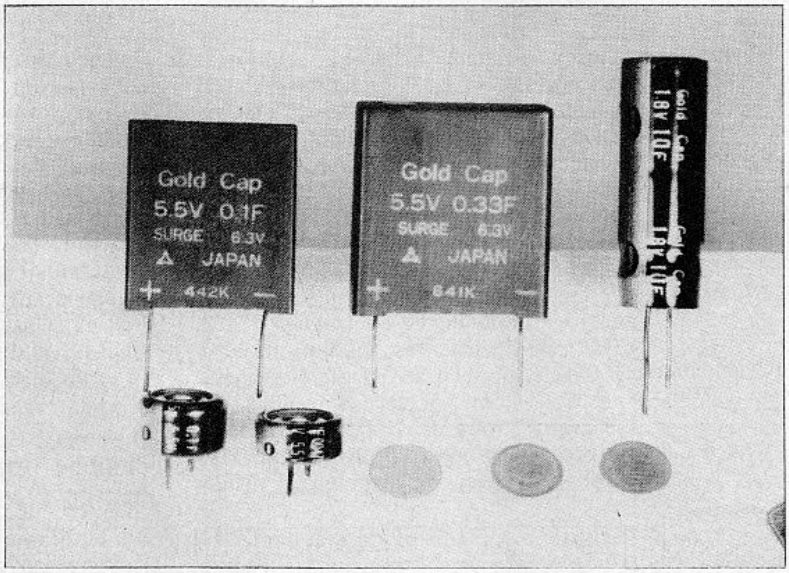
However, the laser to which he had access produced a spot 10 μm across, far too large when the chip has features that are only 2 μm or 3 μm apart. An electron beam would have eroded the metal, but the 1 keV of energy necessary would have destroyed the rest of the chip. The only option was an ion beam and that meant going to OAR.

Fabulous machine

OAR used a machine it had developed with the Science and Engineering Research Council and which was sited in the Engineering Science Department of Oxford University. The repair work saved STC six weeks and a lot of money. Dr Clampitt has identified a two-tier market for OAR. "I can see us setting-up a chip repair shop in the United Kingdom for the small boys and selling machines to the big chip companies who have chips diagnostic equipment in their laboratories.

"We have made a fabulous machine and what I want to do now is go into production."

THE SUPER CAPACITOR: OPERATION AND APPLICATION



Power supply back-up capacitors with a capacitance between several tens of milli-farads and tens of farads are currently available from a number of manufacturers. In spite of their huge capacitance, these devices are physically very small with sizes varying between that of a button cell and a matchbox.

The use of CMOS memory elements in combination with a back-up battery to give a non-volatile memory is fairly standard these days. But non-rechargeable batteries often go flat quite unexpectedly, and the lifetime of NiCd types is also limited. Fortunately, the current consumption of CMOS circuits has been significantly reduced over the past few years, and memories need only be powered from a back-up supply for as long as the main power supply is off, which may last from a few seconds to a few weeks. With this in mind, the choice of the capacitor as a back-up supply is not surprising. However, the size and electrical characteristics of electrolytic types make these unsuitable for practical ap-

plication in a back-up supply. Fortunately, thanks to special techniques, it has become possible to produce a type of capacitor that combines high capacitance with small size. This recent development is known under the name *electric double layer capacitor*, or *super capacitor*. Depending on the type, these capacitors are capable of powering CMOS circuits for periods of several weeks, or even several months.

A special structure

Conductive materials exchange charged particles when brought into contact. In the contact area, dissociation gives rise to a potential difference, called *barrier potential*. This principle is utilized in most types of primary and secondary battery, and thermocouplers. The charges causing the barrier potential concentrate in layers along the imaginary dissociation line between the two materials. One material has a surplus charge of positive ions, the other a surplus charge of negative ions. These two layers are commonly referred to as the *electrochemical double layer*.

To illustrate the basic operation of the super capacitor, Fig. 1 shows a cross-sectional view of the layer between carbon and an electrolyte (e.g. diluted sulphuric acid). The structure of the double layer is similar to that of a capacitor. In principle, all that is required to modify the charge in the double layer is to apply an external voltage across the dissociation layer. In practice, however, care should be taken that the current that would inevitably flow through the conductive materials does not cause an electrochemical reaction. Current flow is prevented by the special internal construction of the super capacitor, which will be discussed below.

The capacitance per unit area of the electric double layer is estimated as high

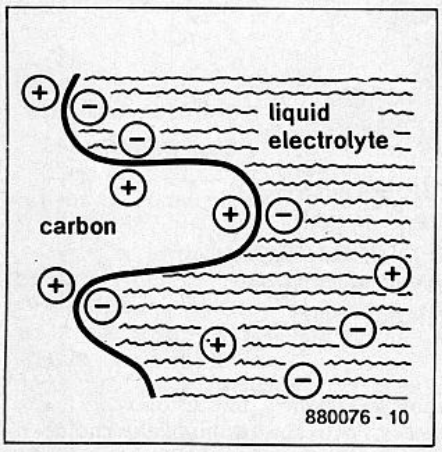


Fig. 1. Electrochemical double layer between two conductive materials.

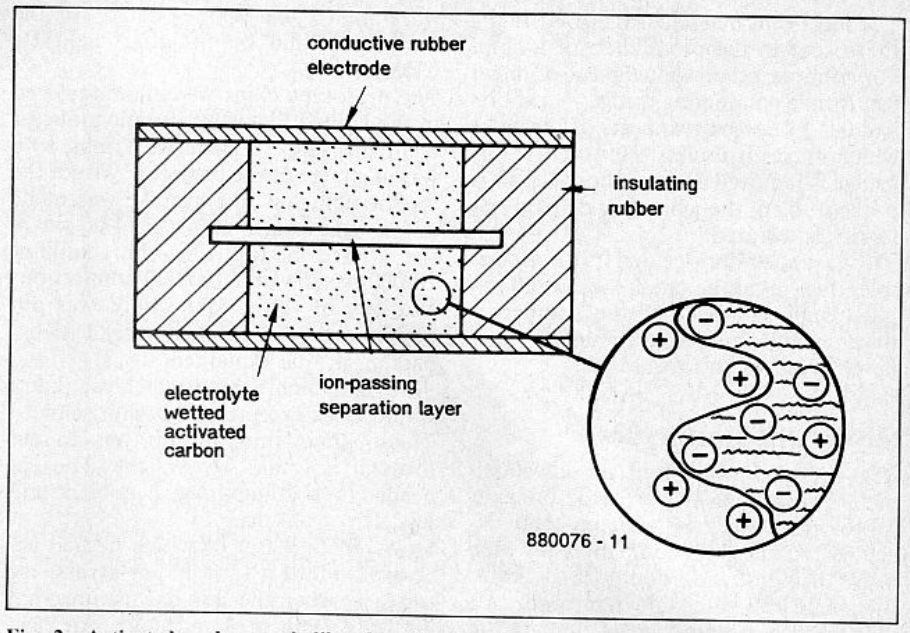


Fig. 2. Activated carbon and diluted sulphuric acid are enclosed in a hermetically sealed package.

as 20 to 40 $\mu F/cm^2$. The previously mentioned carbon is actually *activated carbon*, an extremely porous material whose surface area is of the order of 1000 m^2/g. Consequently, one gram of activated carbon particles can be calculated to provide a capacitance between 200 and 400 farad.

Figure 2 shows the basic construction of the enclosure for the super capacitor. The acidulated, activated, carbon is placed into an insulating rubber gasket which is sealed at both sides with a conductive rubber disc. The unit is closed hermetically by vulcanization. The operation of the cell is enhanced by an thin, ion-permeable, separator, which may be considered a kind of sieve for molecules and ions of a certain size. The separator is dimensioned such that it passes only hydrogen ions in the electrolyte.

The cell operates as follows: when a voltage is applied across the electrodes, positive ions travel through the separator, towards the negative electrode, leaving negative ions behind. This process gives rise to a potential difference across the membrane, and effectively prevents an electrochemical reaction. Meanwhile, the ion balance at both sides of the membrane is lost. An external voltage source, which supplies charge via the negative electrode, and removes charge via the positive electrode, is required to restore the ion balance in the dissociation layer between carbon and electrolyte. Here we have a capacitor with two electrodes and a dielectric.

The capacitor element thus made has a relatively low working voltage (1 to 2 V). For most applications, elements are, therefore, connected in series. Figure 3 shows that stacking is simple to achieve thanks to the basic structure of the super capacitor. The drawing also shows that one terminal is connected to the metal enclosure. Although the capacitor is, strictly speaking, non-polarized, this terminal is usually marked –, and connected to ground.

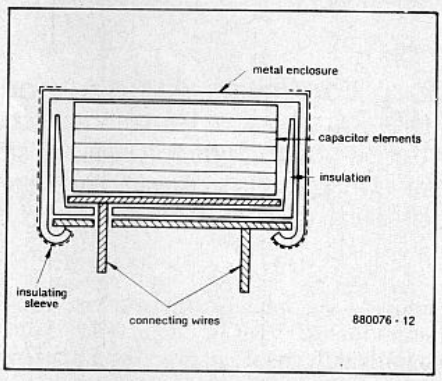


Fig. 3. Increasing the working voltage of the capacitor by series-connection of individual elements.

Electric operation of the double layer capacitor

The basic construction of the super capacitor is once more given in Fig. 4 for describing the equivalent circuit. Each carbon particle, C_n, together with the surrounding diluted acid, forms a small capacitor, connected to one electrode either direct, or via surrounding particles (resistance R_{Cn}). The resistance between the particle and the other electrode depends on the ion flow through the liquid electrolyte and the separator (resistance R_{In}).

The value of the small capacitor is related to the surface of the carbon particle. Th resistance between it and the two electrodes depends on its position in the cell. This analysis forms the basis for

the equivalent circuit drawn in Fig. 5. In this, R_S is the electric resistance of the separator membrane (not to be confused with R_{In}), while R_L stands for the capacitor's leakage resistance. The equivalent circuit thus obtained very nearly resembles the actual state of the super capacitor, but is relatively complex. Fortunately, it can be simplified as shown in Fig. 6. This model shows clearly that the super capacitor may be thought of as composed of a large number of R-C networks, whose values of R and C depend on a number of factors, including the size of the individual carbon particle, and its position with respect to the electrodes.

The electrostatic capacitance of the super capacitor has properties similar to the electric capacity of a battery. This means that the capacitance is fairly difficult to ascertain because values obtained depend on measurement conditions. Usually, capacitance is measured by connecting the super capacitor to an external voltage source via a resistor whose value is large relative to the internal resistance of the capacitor. In this set-up, all elementary capacitors are charged equally, so that the recorded charge curve can be used to deduce the effective capacitance. Measurement of the equivalent series resistance (ESR) of the capacitor is not so simple. Manufacturers of super capacitors provide ESR specifications related to a number of test frequencies. The relatively high ESR values found in the data sheets make clear that the super capacitor is, unfortunately, not suitable for AC applications (smoothing; filter circuits).

In conclusion, the main characteristics of the super capacitor can be summarized as follows:

- high volumetric efficiency;
- maintenance-free, simple to install;
- no need for special charging circuits;
- no short-circuit when the capacitor breaks down — the super capacitor forms an open circuit instead.
- Low risk of explosion thanks to low electrolyte content;
- long life withhout dry-up problems;
- not suitable for filter applications because of relatively high ESR.

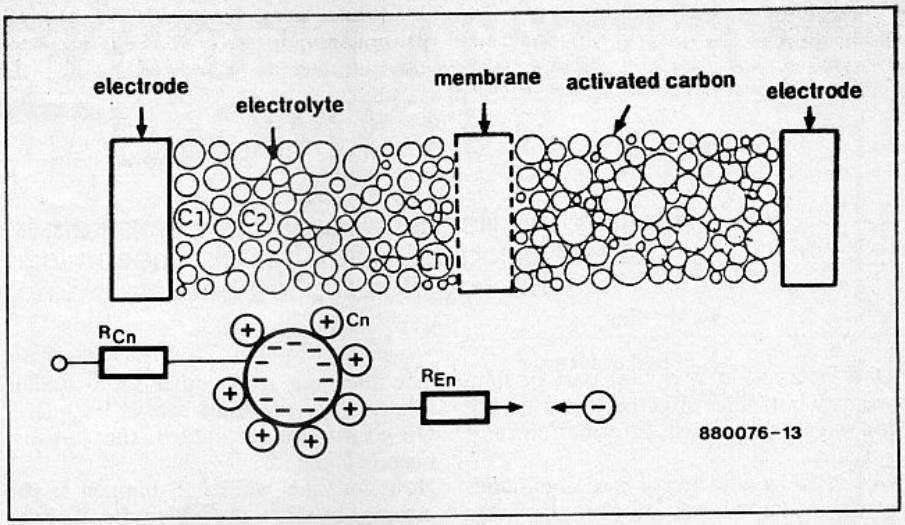


Fig. 4. Cross-section showing the basic structure of the double-layer capacitor.

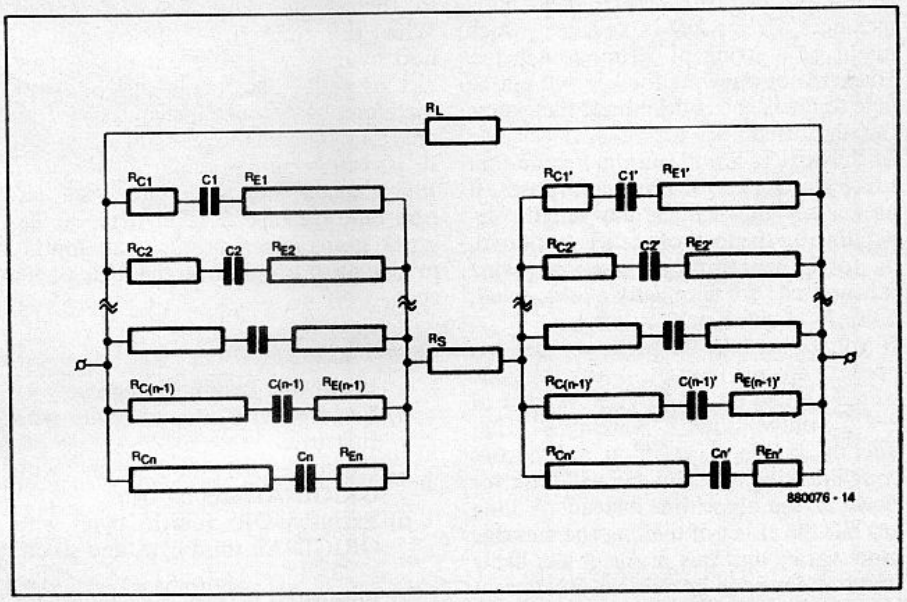


Fig. 5. Equivalent circuit of the super capacitor.

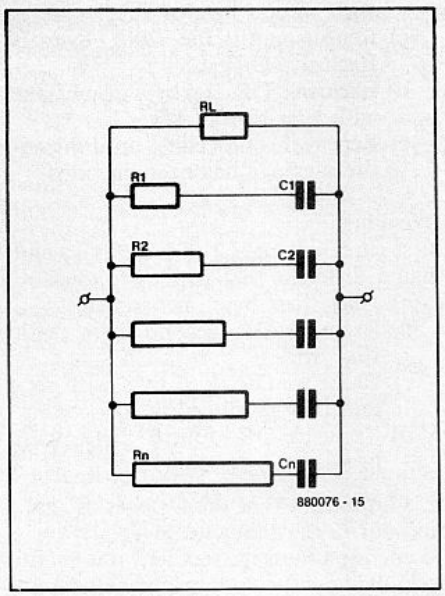


Fig. 6. Simplified equivalent circuit of the super capacitor.

DATA ENCRYPTION

by Pete Chown

Hacking, the illegal accessing of computers, is a crime peculiar to our technological world. It is also becoming more widespread. One way of frustrating hackers is data encryption.

Data encryption is a vital part of data security but, since effective codes are not too widely advertised, information on it is scarce.

The modern tendency is to design codes where a knowledge of the algorithm used for encoding a message is not sufficient by itself to break the code. In such a system, the people exchanging messages agree a key in advance, which might be a string of 20 random bytes. Hackers not knowing the key will not be able to break the code, even if they know the algorithm.

In this article, I will outline a code that I have developed for private purposes. It uses a key that can be any length, depending on the level of security required, up to the length of the message being transmitted. For simplicity's sake, I will, however, assume a 20-byte key.

If you think that 20 bytes is excessive, because anyone trying to break the code would have to hit on the right key out of 2^{160} combinations, remember that nobody in his right mind approaches code breaking this way. He will look for flaws in the algorithm instead. A long key has the effect of making the message more varied and this makes it less likely that someone will be able to see the right key to use.

In its simplest form, the code is formulated by regarding the message as a sequence of bytes. These would normally be ASCII codes. The first byte of the message is then Exclusive-OR-ed with the first byte of the key, the second byte of the message with the second byte of the key, and so on until the key has been used up. The twenty-first byte of the message is then Exclusive-OR-ed with the first byte of the key. This process continues until the message has been coded completely.

This method of encryption suffers from a huge snag. If the hacker gets the first byte of the key right, he will also get every 20th byte right. This will allow him to build up the key bit by bit. The code is, therefore, refined to prevent this.

Before the message is encoded, it is altered in a way that will make it impossible to recover any of it if it contains any errors. The first byte is left as it is, and the second byte is Exclusive-OR-ed with the first byte and stored as the second byte. The third byte is Exclusive-OR-ed with the original second byte, and so on.

The message is decoded in a similar manner, but the third byte is Exclusive-OR-ed with the second byte that has just been calculated.

Now consider what will happen if the message becomes corrupted, because the key has been guessed, but is partly wrong. Any byte that is wrong will lead to the wrong value being generated. When this is Exclusive-OR-ed with the next byte, it will cause this to be incorrect as well. The whole message will, therefore, be decoded incorrectly, even if only one byte in the key is wrong.

It is worth summarizing the way in which encoding and decoding are carried out, because it is difficult to describe it at the same time as attempting to give some insight into the logic of the code.

Encoding

1. a) Leave first byte unchanged.
   b) Exclusive-OR second byte with first byte.
   c) Exclusive-OR third byte with ORIGINAL second byte.
   d) Exclusive-OR fourth byte with ORIGINAL third byte, and so on.

2. a) Exclusive-OR new first byte with first byte of key.
   b) Exclusive-OR new second byte with second byte of key.
   c) Repeat until the 20th byte is Exclusive-OR-ed.
   d) Exclusive-OR 21st byte of message with first byte of key.
   e) Repeat this procedure until the entire message has been encoded.

Decoding

First carry out part 2 of Encoding, and then a different first part as follows.

1. a) Leave first byte unchanged.
   b) Exclusive-OR second byte with first byte.
   c) Exclusive-OR third byte with second byte produced in b).
   d) Exclusive-OR fourth byte with new third byte, and so on.

It is important that these stages are carried out in the sequence given.

To encode a message securely, it is useful to know how the code might be broken. Many hackers would probably approach this by taking one byte at a time, and arrange it so as to maximize the number of spaces, letters 'e', and so on. Once this is done, the key of a simple code often becomes very obvious. Even if it does not, it is possible, by judicious juggling, to discover the key eventually.

In code breaking, the perpetrator can only go so far with his knowledge of the algorithm, and must then rely on educated guesses. In this, he will make use by a knowledge of what characters are most likely to occur. Note that, in pure text, the most common character is a space, not the letter 'e'. As well as letter frequency, there are other considerations that help him. For example, doubled letters give good clues, because very few letters are found in pairs. The same is true of reversed letters: both 'er' and 're', for instance, are common.

The letters of the alphabet in order of frequency of use (in the English language) are:

ETAONRISHDLFCMUGYPWBVKXJQZ

The most common reversed letters are:

RE-ER; ES-SE; AN-NA; TI-IT; ON-NO.

The most common doubled letters, in order of frequency of use, are:

L; E; S; O; T; F; R; N; P; C.

The most common pairs of letters are:

TH; HE; AN; RE; ER; IN; ON; AT; ND; ST; ES; EN; OF; TE; ED; OR; TI; HI; AS; TO.

Readers interested in reading further about this fascinating subject are referred to the following works.

(1) Shannon, Claude E.; *Communications Theory of Secrecy Systems.* Bell System Technical Journal, volume 28 (1949).

(2) Friedman, William F.; *Elements of Cryptanalysis.* Aegean Park Press: U.S.A. (1976).

(3) *Data Encryption Standard.* FIPS PUB 46 National Bureau of Standards, Washington D.C., U.S.A. (1977).

(4) Rivest, R.L. and Shamir, A. and Adleman, J.; *A Method for obtaining Digital Signatures and Public Key Cryptosystems.* Communications of the ACM, volume 26, number 1 (1983).

CONTACT ENCODER AS DIGITAL POTENTIOMETER

The number of so-called autonomous, or stand-alone, applications found for microprocessors and microcontrollers increases daily with the introduction of new equipment. Dishwashers, small household utensils, cameras, test and measurement equipment, and cars, to mention but a few examples, now have some type of built-in microprocessor that affords ease of operation to the user. The microcontroller-driven power supply discussed in Ref. [1] is a good example of how advanced digital electronics can be incorporated into an otherwise analogue test instrument.
Inevitably, where a microprocessor is used, the need arises to provide a reliable user interface. Function keys are adequate as long as the required controls are relatively simple (e.g., the on/off switch). A problem arises, however, when an analogue value is to be set (e.g., volume or tone control on an AF amplifier). A keyboard is not suitable for this. Not entirely unsuitable, but rather inconvenient, is a control based on up/down keys — consider the limited resolution and the time needed to reach the wanted setting. Yet another alternative, the potentiometer followed by an analogue-to-digital converter (ADC), is less attractive from a point of view of cost. The accuracy of the adjustment is limited by the travel of the potentiometer spindle, and 10-turn types are usually about 10 times as expensive as a standard potentiometer. Also, the parallel data output of the ADC may use up most of the computer's I/O capacity.

Bourns, the well-known manufacturer of a wide range of resistors, presets and potentiometers, have recently introduced the digital contact encoder, which forms an attractive solution to the above problems. The contact encoder looks very much like a potentiometer, but supplies digital signals suitable for reading by a microprocessor. The part is essentially a rotary switch without an end-stop. The output signals are phase-shifted as a function of rotational operation. The direction of travel of the spindle is deduced from the phase relationship, while the number of pulses is a measure of the magnitude of travel.
Bourns currently offer contact encoders with 12, 24 or 36 discrete spindle positions (*detents*) per revolution, and 6, 9, 12 or 24 cycles of the output signal, again, per revolution. The choice between these types will be governed by requirements as to ease of setting the relevant control, and the number of steps (for applications involving a large number of steps, it is often desirable to use a contact encoder that supplies relatively many cycles per revolution).

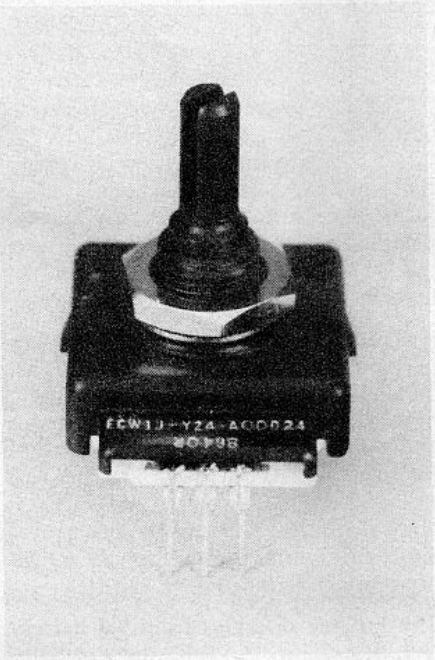
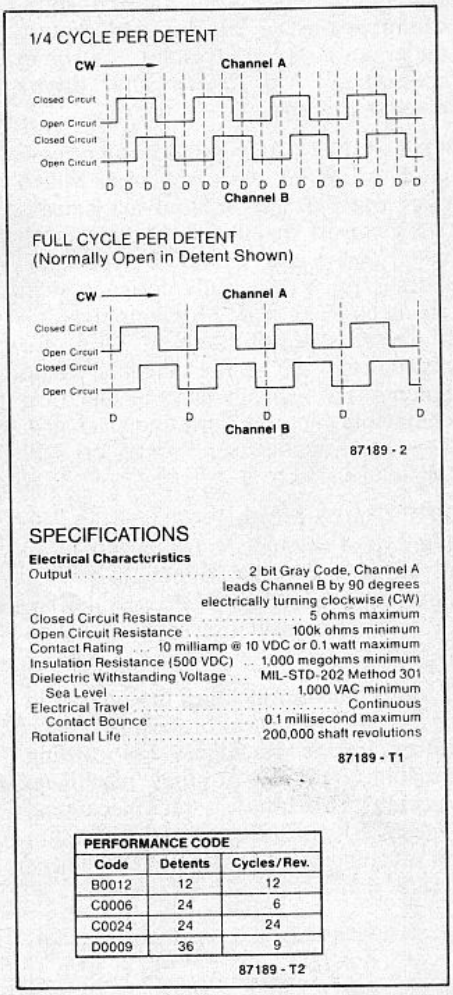


Fig. 1. Very similar to an ordinary potentiometer at first sight, the contact encoder is functionally completely different because it supplies digital signals.

Benefits of the contact encoder are mainly ease of use, simple interfacing circuits, and relatively low cost. Since the contact encoder is basically a pair of switches with a common pole, contact debouncing should be provided in software. In the microcontroller-driven power supply, a Bourns contact encoder is used as the front panel control for setting current and voltage.

Reference:

[1] Microcontroller-driven power supply; Parts 1, 2, 3. *Elektor Electronics* May 1988, June 1988, September 1988.



SPECIFICATIONS

Electrical Characteristics

Output	2 bit Gray Code, Channel A leads Channel B by 90 degrees electrically turning clockwise (CW)
Closed Circuit Resistance	5 ohms maximum
Open Circuit Resistance	100k ohms minimum
Contact Rating	10 milliamp @ 10 VDC or 0.1 watt maximum
Insulation Resistance (500 VDC)	1,000 megohms minimum
Dielectric Withstanding Voltage	MIL-STD-202 Method 301
Sea Level	1,000 VAC minimum
Electrical Travel	Continuous
Contact Bounce	0.1 millisecond maximum
Rotational Life	200,000 shaft revolutions

87189 - T1

PERFORMANCE CODE		
Code	Detents	Cycles/Rev.
B0012	12	12
C0006	24	6
C0024	24	24
D0009	36	9

87189 - T2

Fig. 2. The number of detents and pulses per spindle revolution depend on the type of encoder chosen (*courtesy Bourns*).

Further information on prices and availability of contact encoders is available from:

Bourns Electronics Limited • Hodford House • 12/27 High Street • HOUNSLOW TW3 1TE. Tel.: (01 572) 6531. Telex: 264485.

European Headquarters:
Bourns AG • Zugerstrasse 74 • 6340 Baar • Switzerland. Tel. +41 42 333333. Telex: 868722.

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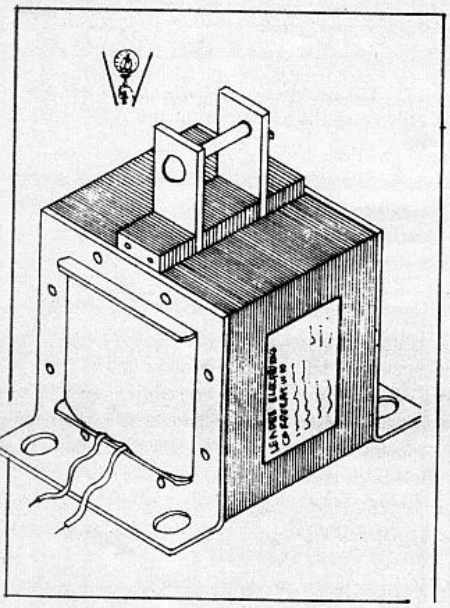

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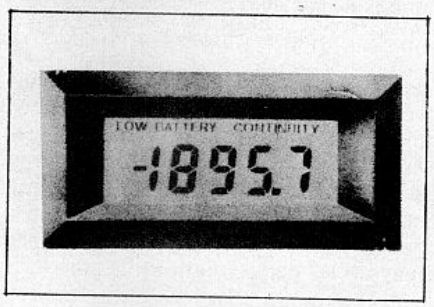
(i) True Digital Hold, (ii) High Accuracy of typically 0.005% ± 1 count (max. 0.01%) achieved by the use of low ppm, high stability BAND GAP Reference and calibration-on in-house standard of 5.5 digit of 0.0015% accuracy, and (iii) Logic Selectable 200 mV or 2 V FSD capable of offering 10 uV resolution. (iv) True differential inputs provide a high noise rejection (CMRR of 110 dB).

The module operates from 9V battery (typically 7.5 to 15 VDC) at a consumption of less than 1 mA. The inputs are protected upto ± 20 VDC.



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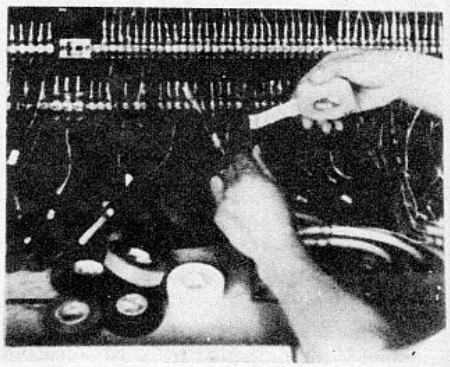

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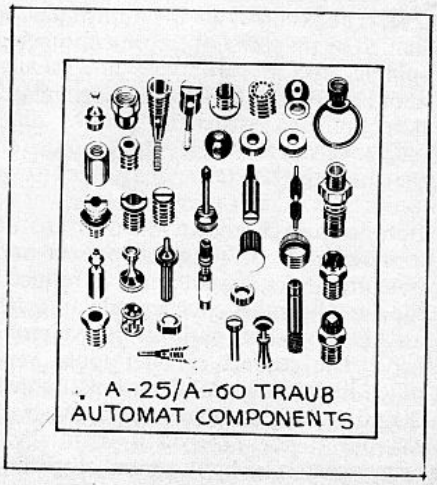

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Transistors & Heatsinks

Electronics is a fine hobby. Reading and understanding the circuit diagrams, trying to figure out why a particular resistance value has been chosen, knowing the functions assigned to different transistors in the circuit, everything works out very well on paper. But as always, theory remains theory. It really becomes interesting and challenging when the circuit is constructed and it finally "Works" as desired.

In case of SELEX projects, we have always been giving special attention to the construction part. These hints and tips have been given again and again to help the newcomers to this hobby. The component placement is very important and the sequence of assembling is also equally important. A newcomer needs to be reminded about the polarity of capacitors and diodes every now and then.

The marking of pin number 1 on ICs is also an important thing to remember. Equally important are the pin out diagrams of various ICs and transistors. Every thing is simple, but important.

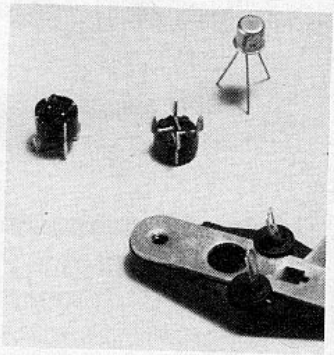
Speaking of transistors, apart from the pin details, we must also give proper attention to the heat dissipation. A transistor has a ratted heat-dissipation capacity, and if the generated heat is more than what it can dissipate on its own, we must provide some assistance. This task is assigned to heat sinks. As the name itself suggests.... these are provided for sinking the extra heat that may be generated, and to keep the transistors well within their specified operating temperature range. The extra heat can also be generated by the adjacent components on the PCB, and can affect transistor performance. One way to avoid this is to mount the transistors away from devices which may generate and radiate heat. Change in temperature can influence the functioning of the transistor, because the semiconductor junctions are sensitive to heat. If the temperature rises beyond the rated maximum value, the transistor itself may be destroyed. This is true, not only in case of a transistor working in the circuit, but also in case of a transistor being soldered in its place.

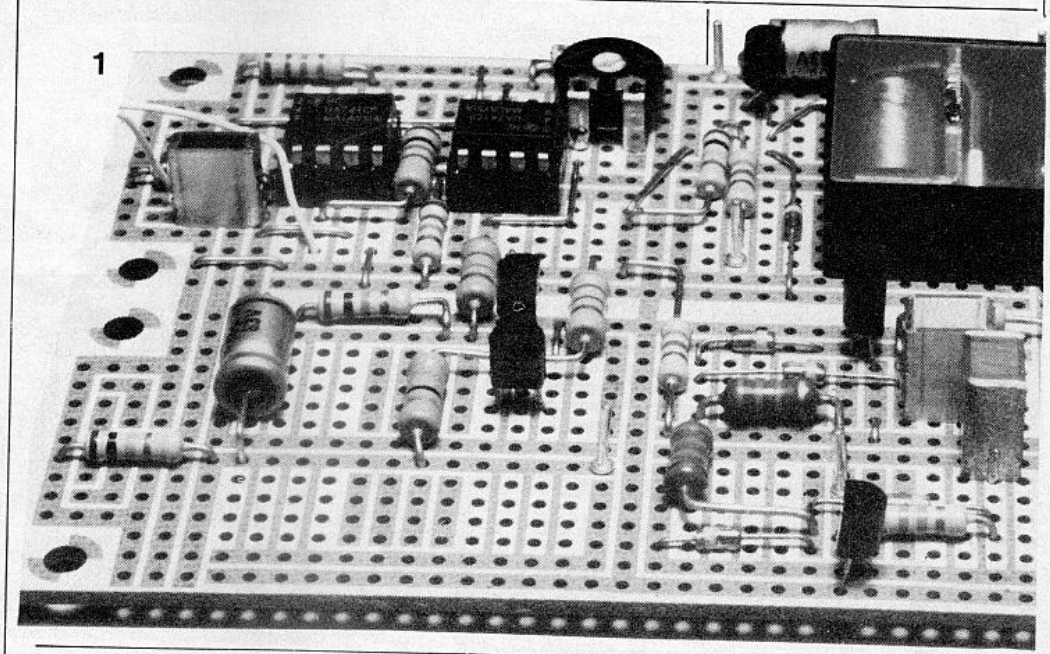
A general overview of soldering temperatures and soldering periods is given below:

Transistor Casing.	Soldering Temperature	Distance between casing and Soldering tip	Maximum Soldering Period
Metal	Upto 250°C Upto 250°C 250°C to 350°C	1.5 to 5 mm Above 5 mm Above 5 mm	5 Sec. 10 sec. 5 sec.
Plastic	Upto 250°C Upto 250°C	2 to 5 mm Above 5 mm	3 Sec. 5 Sec.

Figure 1:
The transistors in TO-92 package. The small ones, which need no heat sinks.

Figure 2:
Transistor sockets and pad.





1

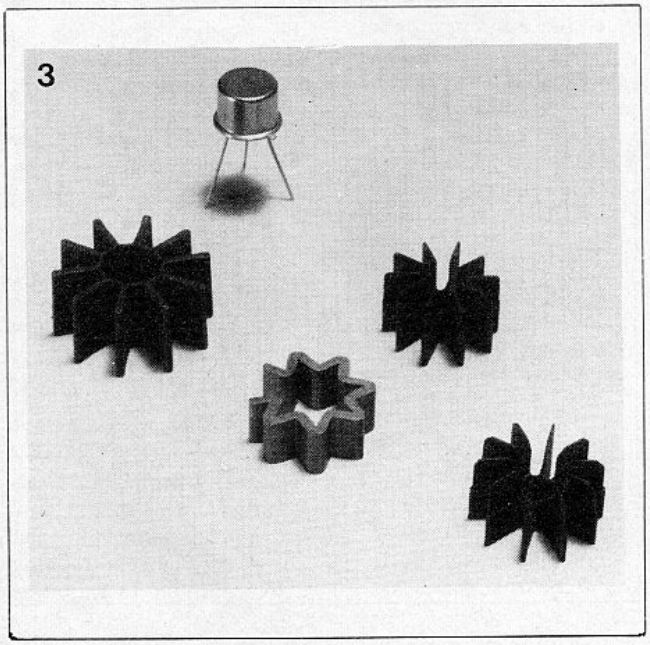
Mounting sockets are generally not used for the transistors, but a few types of sockets and insulating bases are available, which are shown in figure 2. These are provided with insulating bodies and with pins. Spring clamps can also be provided in some designs, to hold the transistor in place.

Heat Sinks:

Every transistor has a rated heat dissipation capacity and a rated working temperature. These two are closely related. Cooling fins and heat sinks are required whenever the transistor approaches its rated dissipation capacity. This helps in bringing down the temperature of the transistor without cutting down its power handling capacity. Transistors with round metal can casings are generally fitted with cooling fins. Some types of cooling fins are shown in figure 3.

These fins are designed to have a grip over the transistor casing and provide full contact with the casing surface. This contact effectively helps in increasing the heat dissipating surface area, and in turn helps in bringing down the temperature of the transistor.

In case of transistors with plastic casings in SOT-32 and TO-220, a mettalic backing is provided with a hole for fixing it to a heat sink. If the transistor is used much below its specified ratings, then this metalic backing itself is enough to dissipate the heat. However, when the transistor is being used at its normal ratings, it is advisable to use a heatsink as shown in figure 4. The metallic backing must face the heatsink surface, when mounting it onto the heatsink. The metalic backing is generally connected to the collector of the transistor, and should be electrically isolated from other parts in the circuit. An unwanted short circuit may damage the transistor. As the heatsink is directly screwed on to this metallic surface, the heat sink should



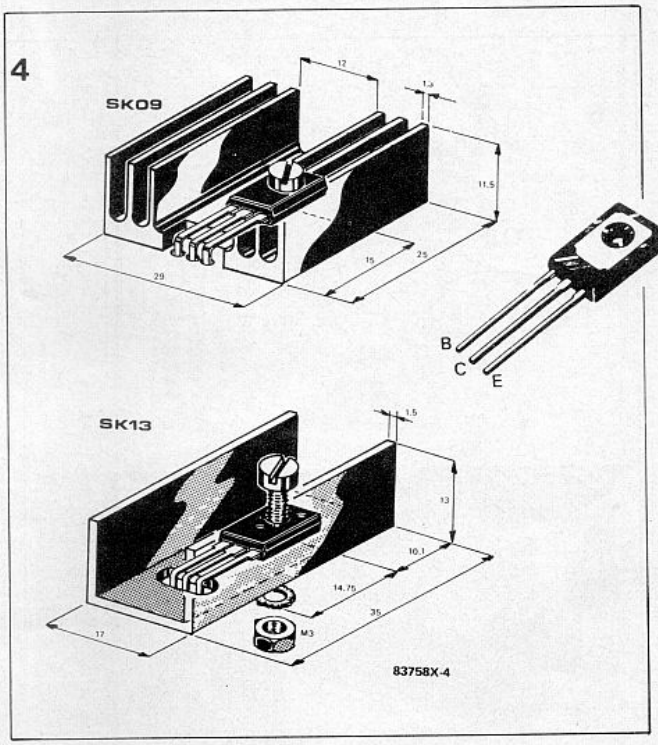
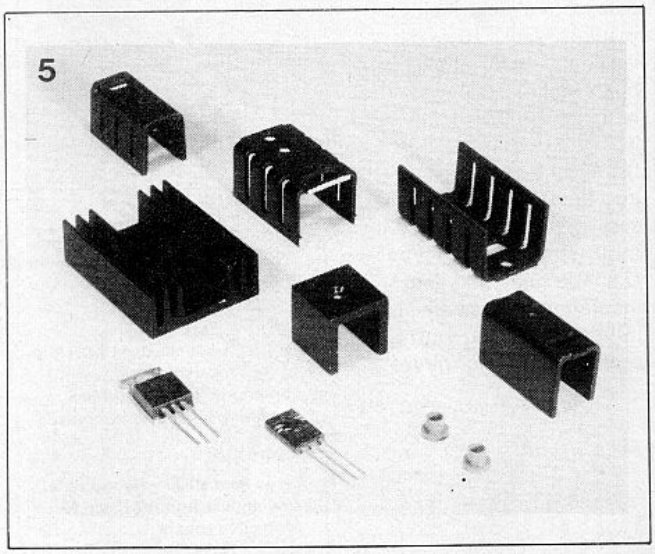


Figure 3:
Different types of cooling fins to be directly pushed over the transistor body.

Figure 4:
Heat Sinks used with TO-20 and SOT-32 type transistor casings. A Mica lamination must be placed between the transistor body and the heat sink surface.

Figure 5:
U section heat sinks, with insulating bushes and transistors.



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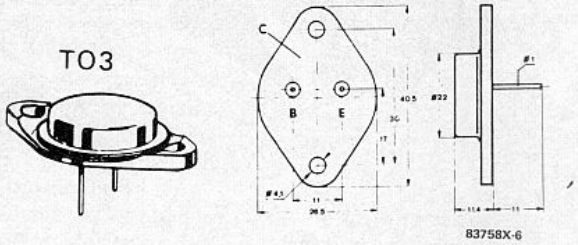

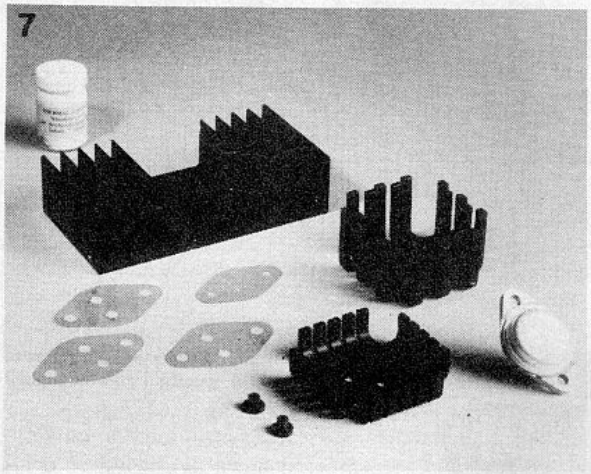

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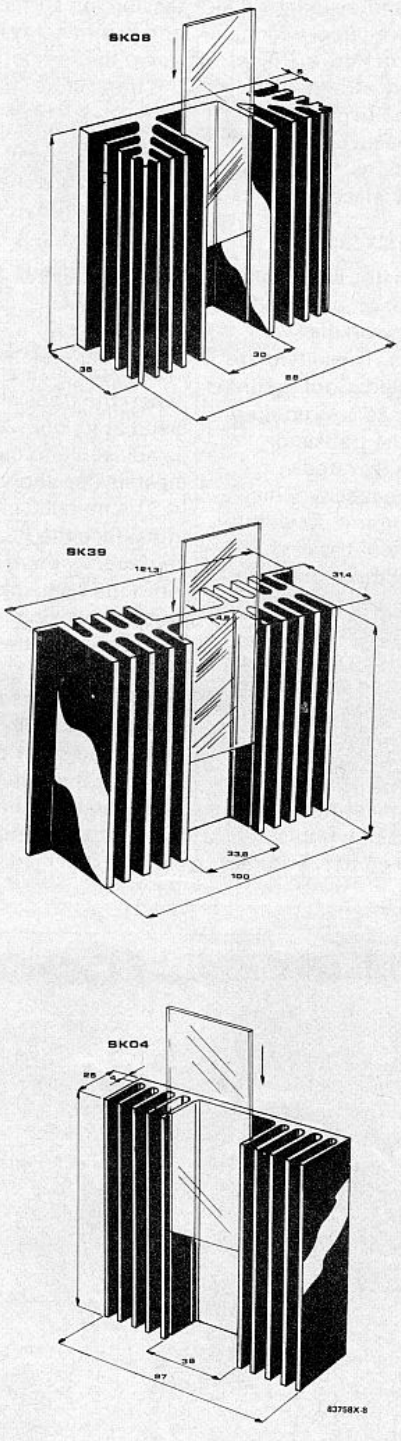


also be properly isolated. If this becomes impossible, the transistor body must be electrically isolated from the heat sink, with thermally conductive electrical insulators, like Mica laminations. An insulating bush also must be inserted with the mounting screw, to isolate the mounting screw from the transistor body and the heatsink. A nylon screw can also be used for mounting. Different types of U shape heatsinks and insulating bushes are shown in figure 5, along with two types of transistor packages.

Figure 6:

TO-3 package of the well known 2N 3055 power transistor.

Figure 7:

Larger heat sinks used with high power transistor. Heat sink compound (paste) and Mica insulating laminates is a must.

Figure 8:

Large heat sinks with multiple cooling fins, and provision for protective covers.

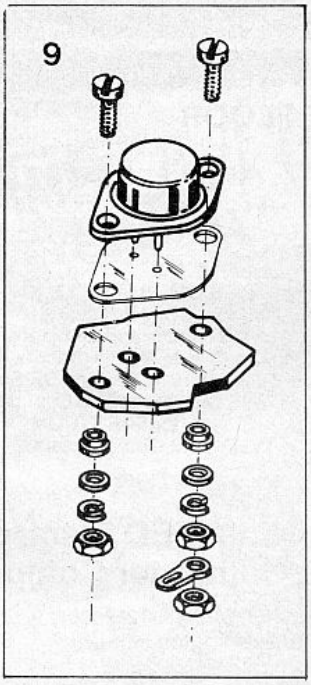
Power transistors in T0-3 casing, like the 2N 3055, also need heat sinks. In case of powers upto 20 W, simple small heatsinks as shown in figure 7 are adequate. Figure 7 also shows the Mica laminations and insulating bushes which must be used with the heatsinks.

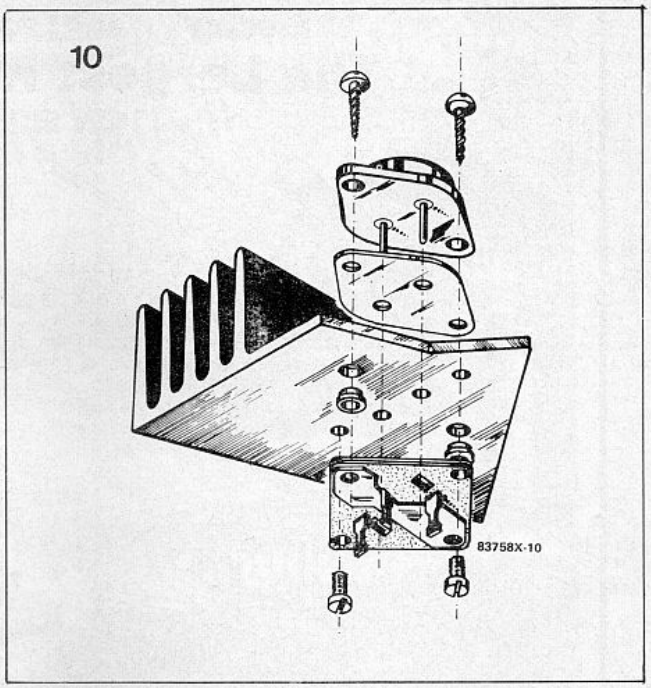
In case of higher power handling requirements, the transistors must be mounted on larger heatsinks with multiple cooling fins in various configurations, as shown in figure 8. Whenever a pair of power transistors is being used together, it is preferable to mount both the transistors on the same heat sink body. This helps in maintaining both the transistors at same temperature.

Mounting holes are generally provided on standard heat sinks, but if the extruded heat sink is purchased in higher lengths, for cutting to required size in future, proper mounting holes must be drilled into these pieces. Figure 6 gives the drilling dimensions for a TO-3 casing.

Whenever larger and heavier heat sinks are used, they are generally mounted on the chassis or the equipment enclosure itself. In such a case, the enclosure and the chassis may be connected to earth. It is most important to isolate the transistor body, which is also the collector connection of the transistor, from the heat sink. Otherwise the collector would be directly short circuited to the earth.

Figure 9 shows an exploded view of the assembly of TO-3 transistors onto heat-sink. Figure 10 shows the assembly when using a socket instead of direct soldering of the transistor.





The exploded view is much more clear than describing the mounting procedure in a number of words.

The heat sinks can be mounted outside or inside the enclosure. If they are mounted on the outside wall of the enclosure, the cooling will be more efficient. If they are mounted inside the enclosure, it is better to provide ventilation holes below and above the place where the heat sink is mounted inside. A vertical heat sink always provides better cooling because of improved circulation.

Insulating strips as shown in figure 8, or insulating caps as shown in figure 11 can be used for increased isolation of the transistor.

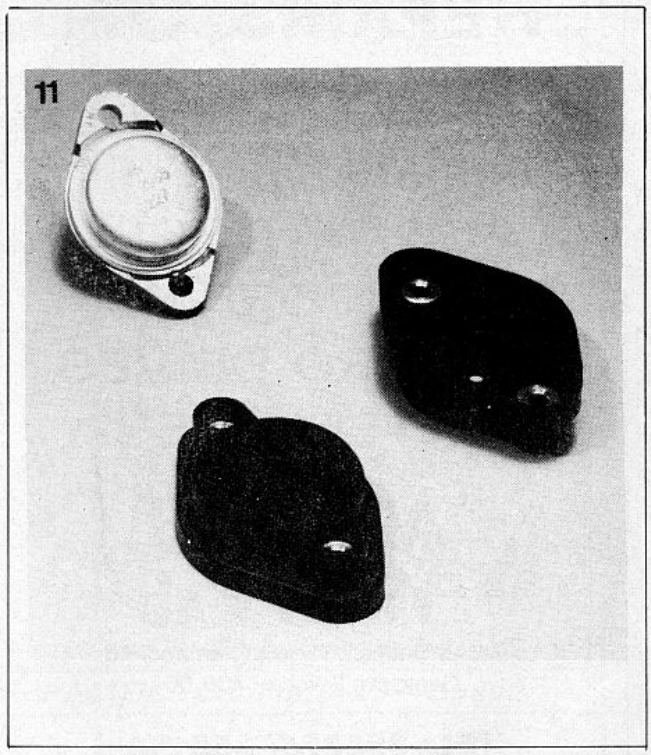
Some more points to remember are –

1. Use a good heat sink compound (paste) between the transistor body, mica plate and heat sink surface.
2. Use insulating sleeves over the soldered joints at the transistor pins.
3. Check for proper insulation between the transistor body (collector) and heat sink body.

Figure 9:
Exploded view (without socket)

Figure 10:
Exploded view (with socket used)

Figure 11:
Insulating/protective caps for TO-3 transistors.



CORRECTIONS

Microprocessor-controlled radio synthesizer — 2

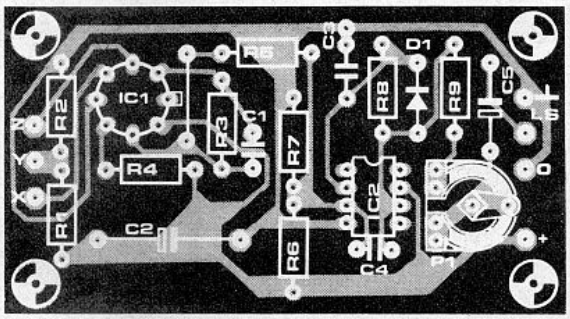
October 1988,

In the circuit diagram of Fig. 9, junction (R57-C29) should be connected to junction (drain T8-L3). The relevant printed circuit board is all right.

Electrometer

August 88 p.8.37

Figure 4 for component layout is printed unreadable The readable layout for the same is given below



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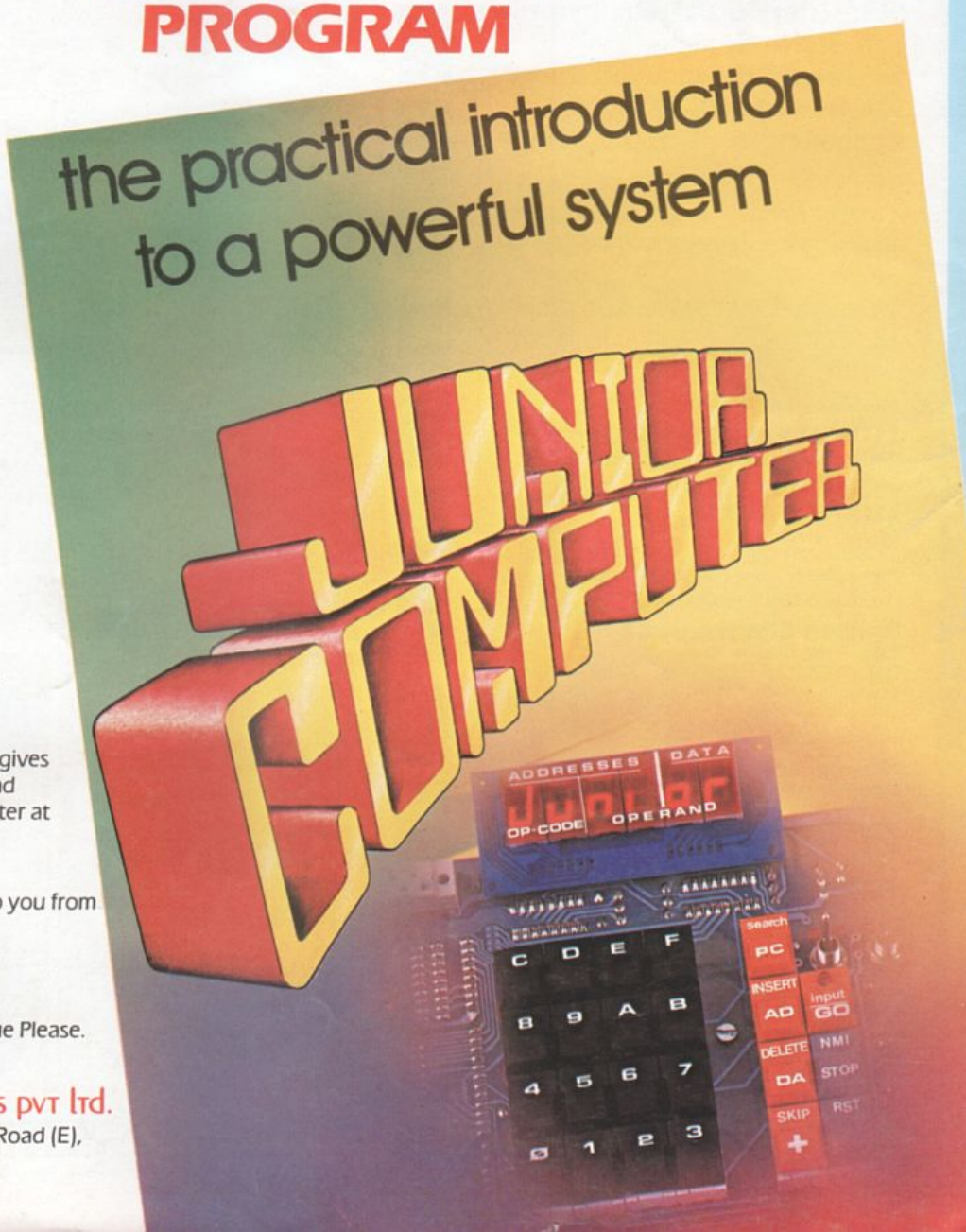

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